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Jameco Part Number 1182395

## 4-Mbit (512K x 8) Static RAM

### Features

- **Very high speed: 45 ns**
  - **Wide voltage range: 2.20V – 3.60V**
- **Pin-compatible with CY62148DV30**
- **Ultra-low standby power**
  - **Typical standby current: 1µA**
  - **Maximum standby current: 7µA (Industrial)**
- **Ultra low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
- **Easy memory expansion with  $\overline{CE}$ , and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Offered in Pb-free 36-ball VFBGA, 32-pin TSOP II and 32-pin SOIC packages**

### Functional Description<sup>[1]</sup>

The CY62148EV30 is a high-performance CMOS static RAMs organized as 512K words by 8 bits. This device features

advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected ( $\overline{CE}$  HIGH).

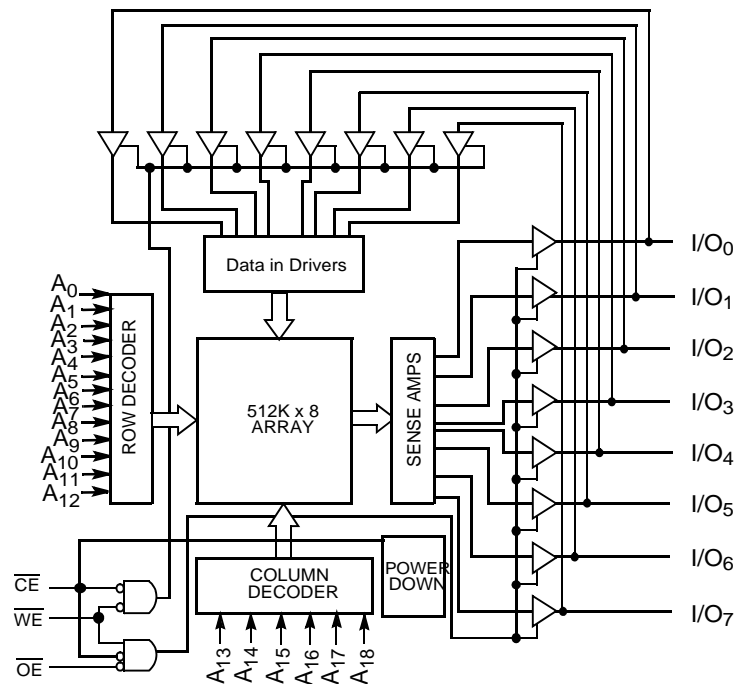
To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY62148EV30 is available in 36-ball VFBGA, 32-pin TSOP II, and 32-pin SOIC packages.

### Logic Block Diagram

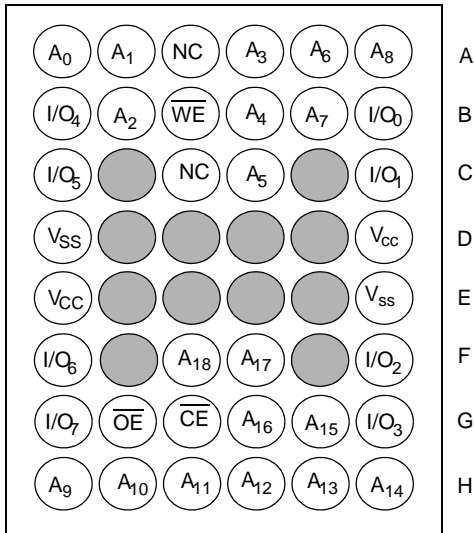


#### Note:

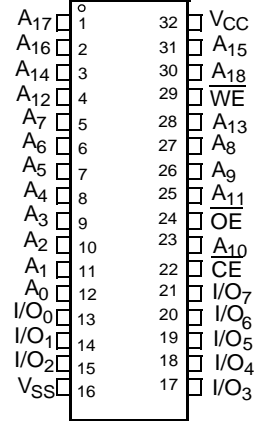
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2]</sup>**

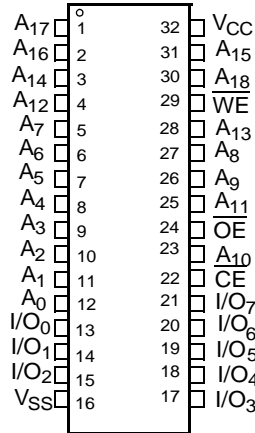
**36-ball VFBGA Pinout**  
**Top View**



**32-pin TSOP II Pinout**  
**Top View**



**32-pin SOIC Pinout**  
**Top View**



**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (uA)	
	Min.	Typ. <sup>[4]</sup>	Max.		f = 1 MHz		f = f <sub>max</sub>			
				Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	
CY62148EV30-45LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7
CY62148EV30-55LL <sup>[3]</sup>	2.2	3.0	3.6	55	2	3	15	25	1	20

**Notes:**

- NC pins are not connected on the die.
- Automotive product information is Preliminary.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... 55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.3V to  $V_{CC(MAX)} + 0.3V$   
 DC Voltage Applied to Outputs in High-Z State<sup>[5,6]</sup> ..... -0.3V to  $V_{CC(MAX)} + 0.3V$   
 DC Input Voltage<sup>[5,6]</sup> ..... -0.3V to  $V_{CC(MAX)} + 0.3V$

Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current..... > 200 mA

### Operating Range

Product	Range	Ambient Temperature	$V_{CC}^{[7]}$	Speed
CY62148EV30	Industrial	-40°C to +85°C	2.2V to 3.6V	45 ns
	Automotive	-40°C to +125°C		55 ns

### Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	45 ns (Industrial)			55 ns (Automotive)			Unit
			Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -0.1\text{ mA}$ , $V_{CC} = 2.20V$	2.0			2.0			V
		$I_{OH} = -1.0\text{ mA}$ , $V_{CC} = 2.70V$	2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 0.1\text{ mA}$ , $V_{CC} = 2.20V$			0.4			0.4	V
		$I_{OL} = 2.1\text{ mA}$ , $V_{CC} = 2.70V$			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = 2.2V$ to $2.7V$	1.8		$V_{CC} + 0.3V$	1.8		$V_{CC} + 0.3V$	V
		$V_{CC} = 2.7V$ to $3.6V$	2.2		$V_{CC} + 0.3V$	2.2		$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage	$V_{CC} = 2.2V$ to $2.7V$	-0.3		0.6	-0.3		0.6	V
		$V_{CC} = 2.7V$ to $3.6V$	-0.3		0.8	-0.3		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-4		+4	$\mu A$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-4		+4	$\mu A$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$ , $V_{CC} = V_{CCmax}$ , $I_{OUT} = 0\text{ mA}$ , CMOS levels		15	20		15	25	mA
		$f = 1\text{ MHz}$		2	2.5		2	3	mA
$I_{SB1}$	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ (Address and Data Only), $f = 0$ (OE and WE), $V_{CC} = 3.60V$		1	7		1	20	$\mu A$
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = 3.60V$		1	7		1	20	$\mu A$

**Notes:**

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75V$  for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100  $\mu s$  ramp time from 0 to  $V_{CC(min)}$  and 200  $\mu s$  wait time after  $V_{CC}$  stabilization.

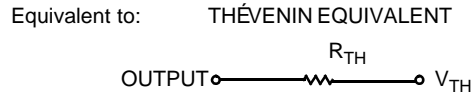
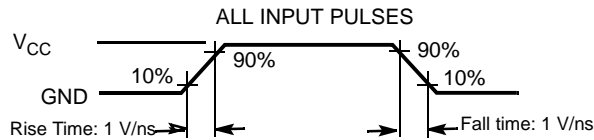
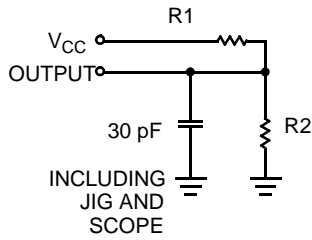
**Capacitance** (For All packages)<sup>[8]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ.)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Thermal Resistance**

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	SOIC Package	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) <sup>[8]</sup>	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	72	75.13	55	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case) <sup>[8]</sup>		8.86	8.95	22	°C/W

**AC Test Loads and Waveforms**

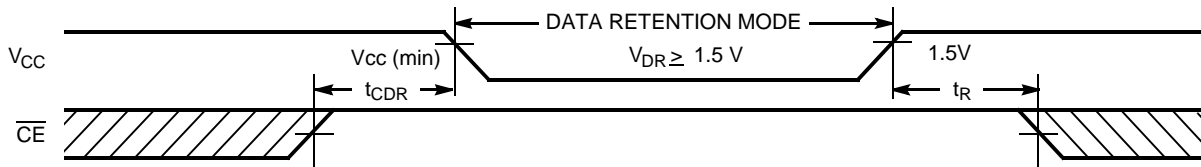


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R <sub>TH</sub>	8000	645	Ω
V <sub>TH</sub>	1.20	1.75	V

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[4]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.5			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.5V, CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	Ind'l	0.8	7	μA
			Auto		12	
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[9]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**



**Notes:**

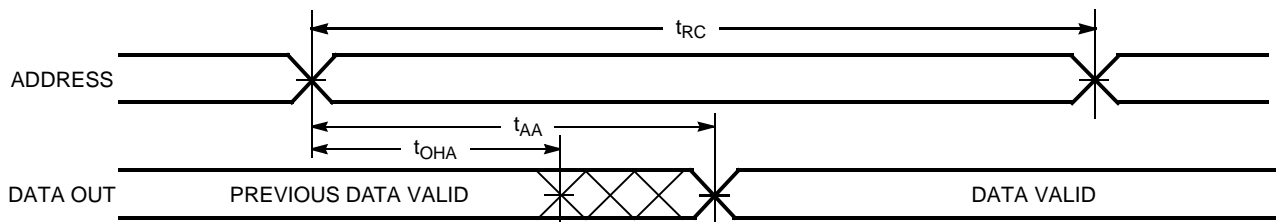
- 8. Tested initially and after any design or process changes that may affect these parameters.
- 9. Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 μs or stable at V<sub>CC(min.)</sub> ≥ 100 μs.

**Switching Characteristics** (Over the Operating Range)<sup>[10]</sup>

Parameter	Description	45 ns		55 ns		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	45		55		ns
t <sub>AA</sub>	Address to Data Valid		45		55	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		45		55	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		22		25	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[11]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[11,12]</sup>		18		20	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[11]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[11, 12]</sup>		18		20	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-up		45		55	ns
<b>Write Cycle<sup>[13]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	45		55		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	35		35		ns
t <sub>AW</sub>	Address Set-up to Write End	35		35		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	35		35		ns
t <sub>SD</sub>	Data Set-up to Write End	25		25		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[11, 12]</sup>		18		20	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[11]</sup>	10		10		ns

**Switching Waveforms**

**Read Cycle No. 1 (Address Transition Controlled)<sup>[14,15]</sup>**

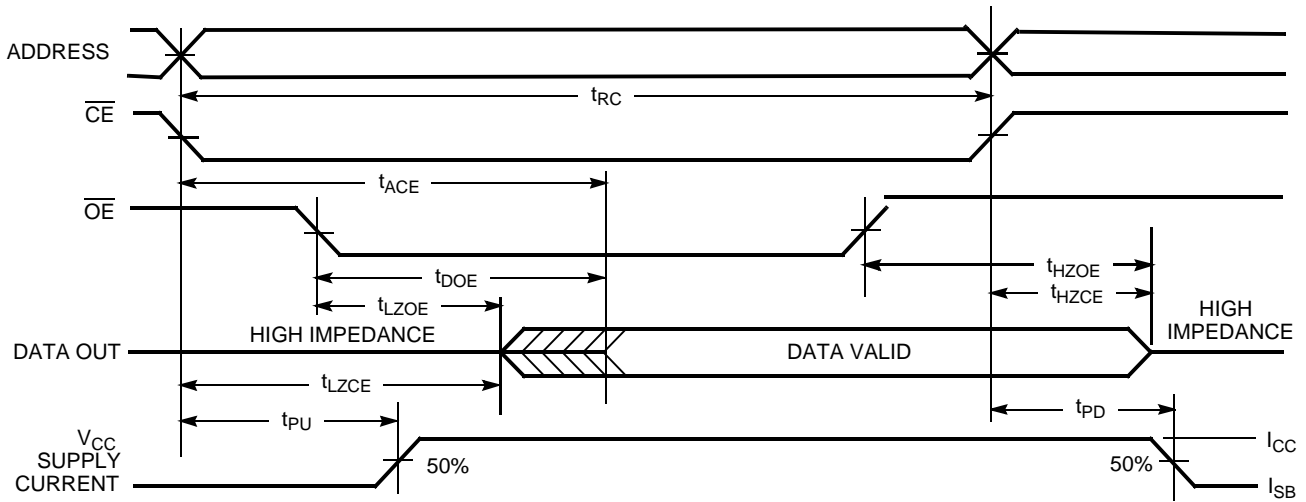


**Notes:**

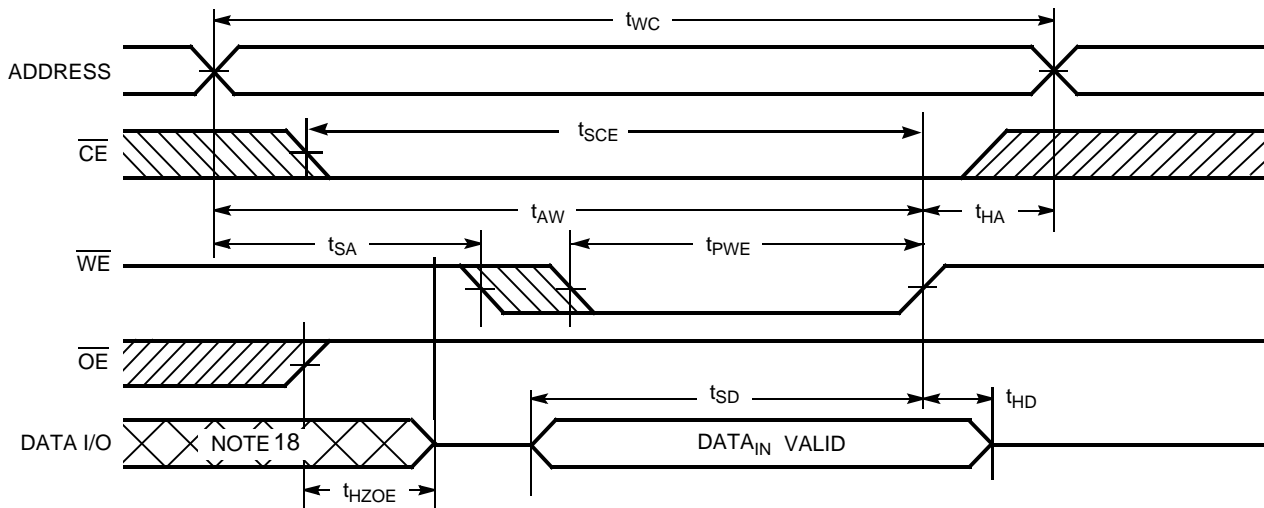
10. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
15.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms** (continued)

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[15,18]</sup>



**Write Cycle No. 1 ( $\overline{WE}$  Controlled)**<sup>[17,19]</sup>

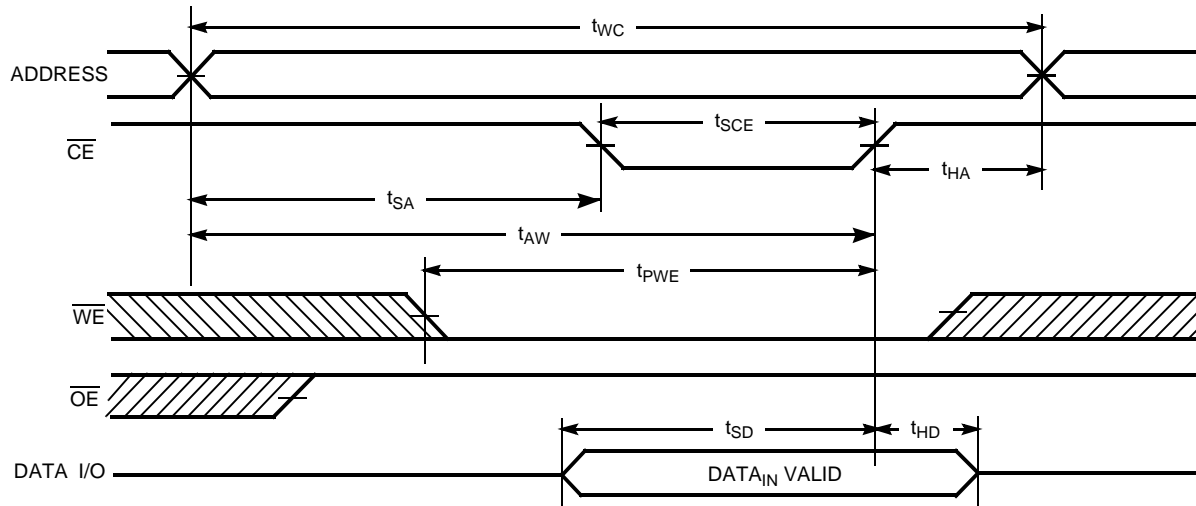


**Notes:**

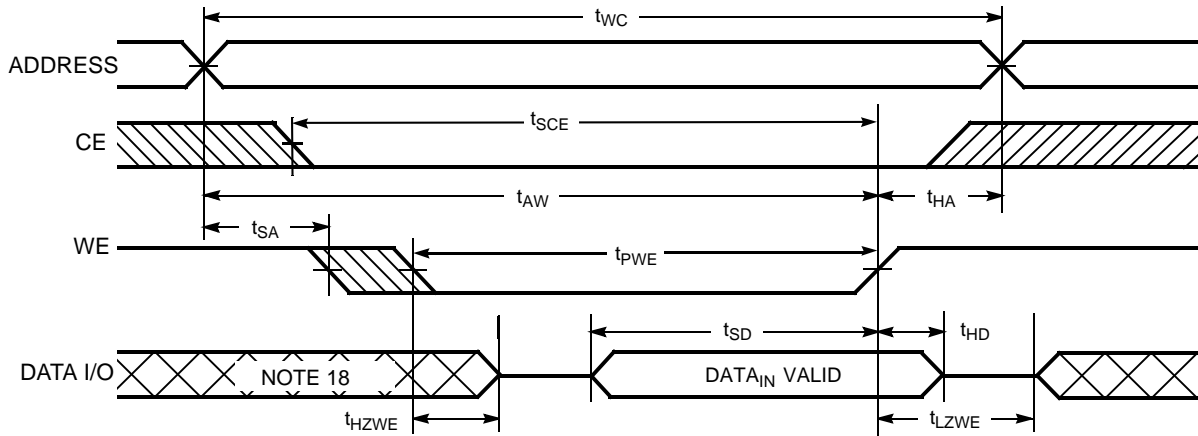
- 16. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 18. During this period, the I/Os are in output state and input signals should not be applied.
- 19. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[17,19]</sup>**



**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[19]</sup>**



**Truth Table**

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	Data Out ( $I/O_0$ - $I/O_7$ )	Read	Active ( $I_{CC}$ )
L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	Data in ( $I/O_0$ - $I/O_7$ )	Write	Active ( $I_{CC}$ )



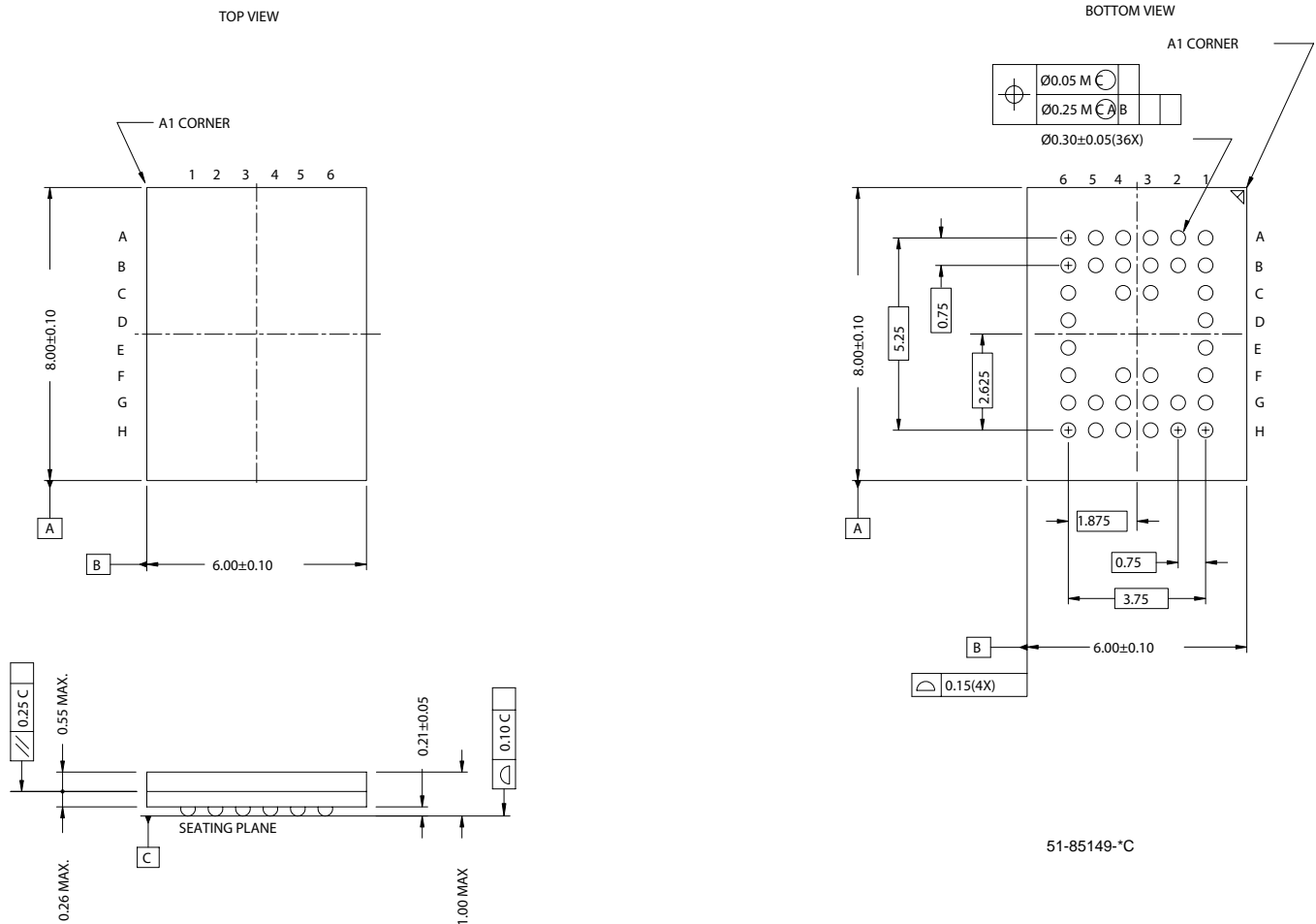
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148EV30LL-45BVXI	51-85149	36-ball Very Fine Pitch Ball Grid Array (Pb-free)	Industrial
	CY62148EV30LL-45ZSXI	51-85095	32-pin Thin Small Outline Package II (Pb-free)	
	CY62148EV30LL-45SXI	51-85081	32-pin Small Outline Integrated Circuit (Pb-free)	
55	CY62148EV30LL-55BVXE	51-85149	36-ball Very Fine Pitch Ball Grid Array (Pb-free)	Automotive
	CY62148EV30LL-55ZSXE	51-85095	32-pin Thin Small Outline Package II (Pb-free)	
	CY62148EV30LL-55SXE	51-85081	32-pin Small Outline Integrated Circuit (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts

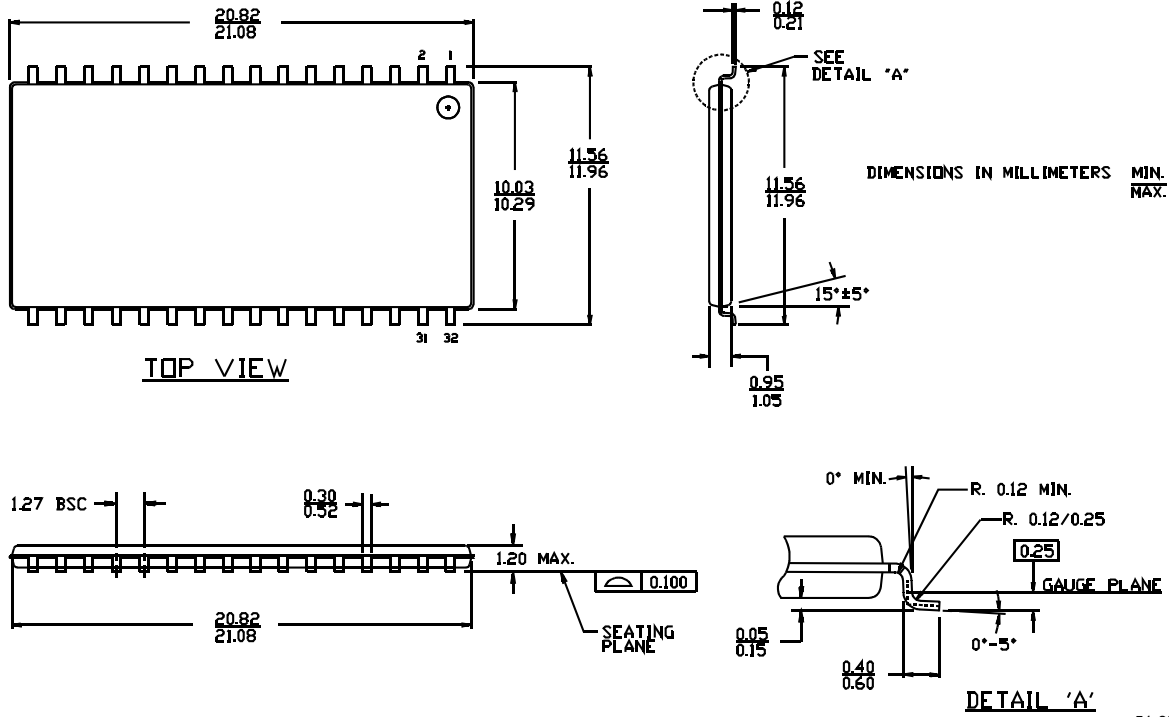
**Package Diagrams**

**36-ball VFBGA (6 x 8 x 1 mm) (51-85149)**



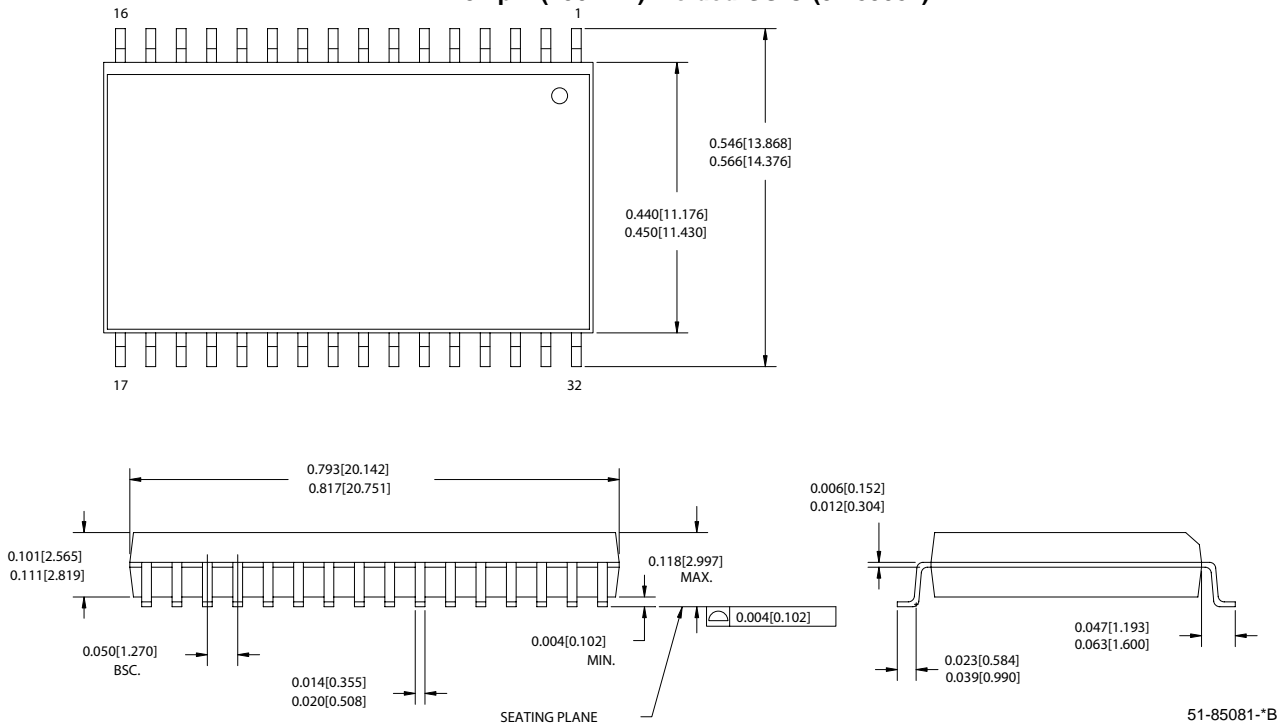
Package Diagrams (continued)

32-Lead TSOP II (51-85095)



51-85095-\*\*

32-pin (450 MIL) Molded SOIC (51-85081)



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**Document History Page**

Document Title: CY62148EV30 MoBL® 4-Mbit (512K x 8) Static RAM				
Document Number: 38-05576				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	223225	See ECN	AJU	New data sheet
*A	247373	See ECN	SYT	<p>Changed from Advance Information to Preliminary            Moved Product Portfolio to Page 2            Changed <math>V_{CC}</math> stabilization time in footnote #7 from 100 <math>\mu</math>s to 200 <math>\mu</math>s            Changed <math>I_{CCDR}</math> from 2.0 <math>\mu</math>A to 2.5 <math>\mu</math>A            Changed typo in Data Retention Characteristics (<math>t_R</math>) from 100 <math>\mu</math>s to <math>t_{RC}</math> ns            Changed <math>t_{OHA}</math> from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin            Changed <math>t_{HZOE}</math>, <math>t_{HZWE}</math> from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin            Changed <math>t_{SCE}</math> from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin            Changed <math>t_{HZCE}</math> from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin            Changed <math>t_{SD}</math> from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin            Changed <math>t_{DOE}</math> from 15 to 18 ns for 35 ns Speed Bin            Changed Ordering Information to include Pb-Free Packages</p>
*B	414807	See ECN	ZSD	<p>Changed from Preliminary information to Final            Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"            Removed 35ns Speed Bin            Removed "L" version of CY62148EV30            Changed ball C3 from DNU to NC.            Removed the redundant footnote on DNU.            Changed <math>I_{CC}</math> (Max) value from 2 mA to 2.5 mA and <math>I_{CC}</math> (Typ) value from 1.5 mA to 2 mA at <math>f=1</math> MHz            Changed <math>I_{CC}</math> (Typ) value from 12 mA to 15 mA at <math>f = f_{max}</math>            Changed <math>I_{SB1}</math> and <math>I_{SB2}</math> Typ. values from 0.7 <math>\mu</math>A to 1 <math>\mu</math>A and Max. values from 2.5 <math>\mu</math>A to 7 <math>\mu</math>A.            Changed the AC test load capacitance value from 50pF to 30pF.            Changed <math>I_{CCDR}</math> from 2.5 <math>\mu</math>A to 7 <math>\mu</math>A.            Added <math>I_{CCDR}</math> typical value.            Changed <math>t_{LZOE}</math> from 3 ns to 5 ns            Changed <math>t_{LZCE}</math> and <math>t_{LZWE}</math> from 6 ns to 10 ns            Changed <math>t_{HZCE}</math> from 22 ns to 18 ns            Changed <math>t_{PWE}</math> from 30 ns to 35 ns.            Changed <math>t_{SD}</math> from 22 ns to 25 ns.            Updated the package diagram 36-pin VFBGA from *B to *C            Added 32-pin SOIC package diagram and pin diagram            Updated the ordering information table and replaced the Package Name column with Package Diagram.</p>
*C	464503	See ECN	NXR	<p>Included Automotive Range in product offering            Updated Thermal Resistance table            Updated the Ordering Information</p>