LMH6503
Wideband, Low Power, Linear Variable Gain Amplifier

General Description
The LMH™ 6503 is a wideband DC coupled differential input voltage controlled gain stage followed by a high-speed current feedback Op Amp which can directly drive a low impedance load. Gain adjustment range is more than 70dB for up to 10MHz. Maximum gain is set by external components and the gain can be reduced all the way to cut-off. Power consumption is 370mW with a speed of 135MHz. Output referred DC offset voltage is less than 350mV over the entire gain control voltage range. Device-to-device Gain matching is within 0.7dB at maximum gain. Furthermore, gain at any V_G is tested and the tolerance is guaranteed. The output current feedback Op Amp allows high frequency large signals (Slew Rate = 1800V/µs) and can also drive heavy load current (75mA). Differential inputs allow common mode rejection in low level amplification or in applications where signals are carried over relatively long wires. For single ended operation, the unused input can easily be tied to ground (or to a virtual half-supply in single supply application). Inverting or non-inverting gains could be obtained by choosing one input polarity or the other.

To further increase versatility when used in a single supply application, gain control range is set to be from −1V to +1V relative to pin 11 potential (ground pin). In single supply operation, this ground pin is tied to a “virtual” half supply. Gain control pin has high input impedance to simplify its drive requirement. Gain control is linear in V/V throughout the gain adjustment range. Maximum gain can be set to be anywhere between 1V/V to 100V/V or higher. For linear in dB gain control applications, see LMH6502 datasheet.

The LMH6503 is available in the SOIC-14 and TSSOP-14 package.

Features
-3dB BW 135MHz
Gain control BW 100MHz
Adjustment range (typical over temp) 70dB
Gain matching (limit) ±0.7dB
Slew rate 1800V/µs
Supply current (no load) 37mA
Linear output current ±75mA
Output voltage (R_L = 100Ω) ±3.2V
Input voltage noise 6.6nV/√Hz
Input current noise 2.4pA/√Hz
THD (20MHz, R_L = 100Ω, V_O = 2V pp) −57dBc
Replacement for CLC522

Applications
- Variable attenuator
- AGC
- Voltage controller filter
- Multiplier

Typical Application

Gain vs. V_G for Various Temperature

Typical Application

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### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance: (Note 4)
- Human Body: 2kV
- Machine Model: 200V
- Input Current: ±10mA
- \( V_{IN} \) Differential: ±(\( V^+ - V^- \))
- Output Current: 120mA (Note 3)
- Supply Voltages (\( V^+ - V^- \)): 12.6V
- Voltage at Input/Output pins: \( V^+ +0.8V, V^- -0.8V \)

Soldering Information:
- Infrared or Convection (20 sec): 235°C
- Wave Soldering (10 sec): 260°C
- Storage Temperature Range: −65°C to +150°C
- Junction Temperature: +150°C

### Operating Ratings (Note 1)

- Supply Voltages (\( V^+ - V^- \)): 5V to 12V
- Temperature Range: −40°C to +85°C
- Thermal Resistance: \( \theta_{JA} \) \( \theta_{JC} \)
- 14-Pin SOIC: 138°C/W 45°C/W
- 14-Pin TSSOP: 160°C/W 51°C/W

### Electrical Characteristics (Note 2)

Unless otherwise specified, all limits guaranteed for \( T_J = 25°C, V_S = \pm 5V, A_{V(\text{MAX})} = 10, V_{CM} = 0V, R_F = 1k\Omega, R_G = 174\Omega, V_{IN\_DIFF} = \pm 0.1V, R_L = 100\Omega, V_G = +1V \). **Boldface** limits apply at the temperature extremes.

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<th>Conditions</th>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>BW</td>
<td>-3dB Bandwidth</td>
<td>( V_{OUT} &lt; 0.5PP ) ( V_{OUT} &lt; 0.5PP, A_{V(\text{MAX})} = 100 )</td>
<td>135</td>
<td>MHz</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>( V_{OUT} &lt; 0.5PP )</td>
<td>50</td>
<td>MHz</td>
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<tr>
<td>GF</td>
<td>Gain Flatness</td>
<td>( V_{OUT} &lt; 0.5V_{PP}, -1V &lt; V_G &lt; 1V, \pm 0.2dB )</td>
<td>40</td>
<td>MHz</td>
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<tr>
<td>Att. Range</td>
<td>Flat Band (Relative to Max Gain)</td>
<td>( \pm 0.2dB ) Flatness, ( f &lt; 30MHZ )</td>
<td>20</td>
<td>MHz</td>
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<td></td>
<td>Attenuation Range (Note 13)</td>
<td>( \pm 0.1dB, f &lt; 30MHZ )</td>
<td>6.6</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>BW Control</td>
<td>Gain Control Bandwidth</td>
<td>( V_G = 0V ) (Note 11)</td>
<td>100</td>
<td>MHz</td>
<td></td>
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<tr>
<td>PL</td>
<td>Linear Phase Deviation</td>
<td>DC to 60MHz</td>
<td>1.6</td>
<td>deg</td>
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<tr>
<td>G Delay</td>
<td>Group Delay</td>
<td>DC to 130MHz</td>
<td>2.6</td>
<td>ns</td>
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<tr>
<td>CT (dB)</td>
<td>Feed-through</td>
<td>( V_G = -1.2V, 30MHZ ) (Output Referred)</td>
<td>−48</td>
<td>dB</td>
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<td>GR</td>
<td>Gain Adjustment Range</td>
<td>( f &lt; 10MHz )</td>
<td>79</td>
<td>dB</td>
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<td></td>
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<td>( f &lt; 30MHz )</td>
<td>68</td>
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<td><strong>Time Domain Response</strong></td>
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<tr>
<td>( t_r, t_f )</td>
<td>Rise and Fall Time</td>
<td>0.5V Step</td>
<td>2.2</td>
<td>ns</td>
<td></td>
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<tr>
<td>OS%</td>
<td>Overshoot</td>
<td>0.5V Step</td>
<td>10</td>
<td>%</td>
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<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>4V Step (Note 5)</td>
<td>1800</td>
<td>V/( \mu )s</td>
<td></td>
<td></td>
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<tr>
<td>( \Delta G ) Rate</td>
<td>Gain Change Rate</td>
<td>( V_{IN} = 0.3V, 10%—90% ) of final output</td>
<td>4.6</td>
<td>dB/( \mu )s</td>
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<tr>
<td><strong>Distortion &amp; Noise performance</strong></td>
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<td>HD2</td>
<td>2nd Harmonic Distortion</td>
<td>( 2V_{PP}, 20MHz )</td>
<td>−60</td>
<td>dBc</td>
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<td>HD3</td>
<td>3rd Harmonic Distortion</td>
<td>( 2V_{PP}, 20MHz )</td>
<td>−61</td>
<td>dBc</td>
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<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>( 2V_{PP}, 20MHz )</td>
<td>−57</td>
<td>dBc</td>
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<tr>
<td>En tot</td>
<td>Total Equivalent Input Noise</td>
<td>1MHz to 150MHz</td>
<td>6.6</td>
<td>nV/( \sqrt )Hz</td>
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<tr>
<td>I_n</td>
<td>Input Noise Current</td>
<td>1MHz to 150MHz</td>
<td>2.4</td>
<td>pA/( \sqrt )Hz</td>
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<tr>
<td>DG</td>
<td>Differential Gain</td>
<td>( f = 4.43MHz, R_L = 150\Omega, \text{Neg. Sync} )</td>
<td>0.15</td>
<td>%</td>
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<td>DP</td>
<td>Differential Phase</td>
<td>( f = 4.43MHz, R_L = 150\Omega, \text{Neg. Sync} )</td>
<td>0.22</td>
<td>deg</td>
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Electrical Characteristics (Note 2) (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_S = ±5V, A_{V(\text{MAX})} = 10, V_{CM} = 0V, R_F = 1kΩ, R_G = 174Ω, V_{IN-\text{DIFF}} = ±0.1V, R_L = 100Ω, V_G = +1V. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<td>DC &amp; Miscellaneous Performance</td>
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<td>GACCU</td>
<td>Gain Accuracy (see Application Notes)</td>
<td>V_G = 1.0V</td>
<td>+0.25</td>
<td>+0.9/−0.4</td>
<td>dB</td>
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<td></td>
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<td>0V &lt; V_G &lt; 1V</td>
<td>±0.3</td>
<td>+1.3/−1.5</td>
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<td>−0.7V &lt; V_G &lt; 1V</td>
<td>±0.4</td>
<td>+4.4/−4.3</td>
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<td>G Match</td>
<td>Gain Matching (see Application Notes)</td>
<td>V_G = 1.0</td>
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<td>±0.7</td>
<td>dB</td>
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<td></td>
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<td>0 &lt; V_G &lt; 1V</td>
<td>−</td>
<td>+1.7/−1.1</td>
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<td></td>
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<td>−0.7V &lt; V_G &lt; 1V</td>
<td>−</td>
<td>+4.0/−4.7</td>
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<td>K</td>
<td>Gain Multiplier (see Application Notes)</td>
<td>1.58</td>
<td>1.72</td>
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<td>V/V</td>
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<td>1.58</td>
<td>1.91</td>
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<td>V_{CM}</td>
<td>Input Voltage Range</td>
<td>Pin 3 &amp; 6 Common Mode, ICMRRI &gt; 50dB (Note 9)</td>
<td>±2.0</td>
<td>±1.80</td>
<td>±2.2</td>
<td>V</td>
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<tr>
<td>V_{IN-\text{DIFF}}</td>
<td>Differential Input Voltage</td>
<td>Across pins 3 &amp; 6</td>
<td>±0.34</td>
<td>±0.28</td>
<td>±0.37</td>
<td>V</td>
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<td>I_{RG,\text{MAX}}</td>
<td>R_G Current</td>
<td>Pins 4 &amp; 5</td>
<td>±1.70</td>
<td>±1.60</td>
<td>±2.30</td>
<td>mA</td>
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<td>I_{BIAS}</td>
<td>Bias Current</td>
<td>Pins 3 &amp; 6 (Note 7)</td>
<td>11</td>
<td>18</td>
<td>20</td>
<td>µA</td>
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<td>Pins 3 &amp; 6 (Note 7), V_G = ±2.5V</td>
<td>3</td>
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<td>13</td>
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<td>T_{CBIAS}</td>
<td>Bias Current Drift</td>
<td>Pin 3 &amp; 6 (Note 8)</td>
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<td>nA/C</td>
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<td>I_{OFF}</td>
<td>Offset Current</td>
<td>Pin 3 &amp; 6</td>
<td>0.01</td>
<td>2.0</td>
<td>2.5</td>
<td>µA</td>
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<td>T_{C,\text{OFF}}</td>
<td>Offset Current Drift</td>
<td>(Note 8)</td>
<td>5</td>
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<td>nA/C</td>
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<td>R_{IN}</td>
<td>Input Resistance</td>
<td>Pin 3 &amp; 6</td>
<td>750</td>
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<td>kΩ</td>
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<td>C_{IN}</td>
<td>Input Capacitance</td>
<td>Pin 3 &amp; 6</td>
<td>5</td>
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<td>pF</td>
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<tr>
<td>IV_G</td>
<td>V_G Bias Current</td>
<td>Pin 2, V_G = 1.4V (Note 7)</td>
<td>45</td>
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<td>µA</td>
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<td>TC IV_G</td>
<td>V_G Bias Drift</td>
<td>Pin 2 (Note 8)</td>
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<td>nA/C</td>
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<td>R V_G</td>
<td>V_G Input Resistance</td>
<td>Pin 2</td>
<td>70</td>
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<td>kΩ</td>
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<td>C V_G</td>
<td>V_G Input Capacitance</td>
<td>Pin 2</td>
<td>1.3</td>
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<td>pF</td>
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<td>V_{OUT}</td>
<td>Output Voltage Range</td>
<td>R_L = 100Ω</td>
<td>±3.00</td>
<td>±2.97</td>
<td>±3.20</td>
<td>V</td>
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<td>R_L Open</td>
<td>±3.95</td>
<td>±3.90</td>
<td>±4.05</td>
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<td>R_{OUT}</td>
<td>Output Impedance</td>
<td>DC</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
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<td>I_{OUT}</td>
<td>Output Current</td>
<td>V_{OUT} ±4V from Rails</td>
<td>±75</td>
<td></td>
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<td>mA</td>
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<td>V_{O,\text{OFFSET}}</td>
<td>Output Offset Voltage</td>
<td>−1V &lt; V_G &lt; 1V</td>
<td>±80</td>
<td>±350</td>
<td>±380</td>
<td>mV</td>
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<tr>
<td>+PSRR</td>
<td>+Power Supply Rejection Ratio (see (Note 10))</td>
<td>Input Referred, 1V change, V_G = 1.4V</td>
<td>−80</td>
<td>−58</td>
<td>−56</td>
<td>dB</td>
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<tr>
<td>−PSRR</td>
<td>−Power Supply Rejection Ratio (see (Note 10))</td>
<td>Input Referred, 1V change, V_G = 1.4V</td>
<td>−67</td>
<td>−57</td>
<td>−51</td>
<td>dB</td>
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<td>CMRR</td>
<td>Common Mode Rejection Ratio (see (Note 9))</td>
<td>Input Referred, V_G = 1V</td>
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<td>dB</td>
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<td>−1.8V &lt; V_{CM} &lt; 1.8V</td>
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<td>I_S</td>
<td>Supply Current</td>
<td>R_L = Open</td>
<td>37</td>
<td>50</td>
<td>53</td>
<td>mA</td>
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<td>R_L = Open, V_S = ±2.5V</td>
<td>12</td>
<td>20</td>
<td>23</td>
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</table>
Electrical Characteristics (Note 2) (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ > TA.

Note 3: The maximum output current (IOUT) is determined by device power dissipation limitations or value specified, whichever is lower.

Note 4: Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

Note 5: Slew Rate is the average of the rising and falling rates.

Note 6: Typical values represent the most likely parametric norm. Bold numbers refer to over temperature limits.

Note 7: Positive current corresponds to current flowing in the device.

Note 8: Drift determined by dividing the change in parameter distribution at temperature extremes by the total temperature change.

Note 9: CMRR definition: \[ |\frac{\Delta V_{OUT}}{\Delta V_{CM}}|/AV \] with 0.1V differential input voltage. \( \Delta V_{OUT} \) is the change in output voltage with offset shift subtracted out.

Note 10: +PSRR definition: \[ |\frac{\Delta V_{OUT}}{\Delta V^+}|/AV \], -PSRR definition: \[ |\frac{\Delta V_{OUT}}{\Delta V^-}|/AV \] with 0.1V differential input voltage. \( \Delta V_{OUT} \) is the change in output voltage with offset shift subtracted out.

Note 11: Gain Control Frequency Response Schematic:

Note 12: Gain/Phase normalized to low frequency value at each AV.

Note 13: Flat Band Attenuation (Relative To Max Gain) Range Definition: Specified as the attenuation range from maximum which allows gain flatness specified (either ±0.2dB or ±0.1dB), relative to AVMAX gain. For example, for f<30MHz, here are the Flat Band Attenuation ranges:
- ±0.2dB: 10V/V down to 1V/V=20dB range
- ±0.1dB: 10V/V down to 4.7V/V=6.5dB range

Connection Diagram

Ordering Information

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<th>Part Number</th>
<th>Package Marking</th>
<th>Transport Media</th>
<th>NSC Drawing</th>
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<tr>
<td>14-pin SOIC</td>
<td>LMH6503MA</td>
<td>LMH6503MA</td>
<td>55 Units/Rail</td>
<td>M14A</td>
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<tr>
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<td>LMH6503MAX</td>
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<td>2.5k Units Tape and Reel</td>
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<tr>
<td>14-Pin TSSOP</td>
<td>LMH6503MT</td>
<td>LMH6503MT</td>
<td>94 Units/Rail</td>
<td>MTC14</td>
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<td>LMH6503MTX</td>
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<td>2.5k Units Tape and Reel</td>
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</table>

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Typical Performance Characteristics

Unless otherwise specified: \( V_S = \pm 5V, 25^\circ C, V_G = V_{G\_MAX}, V_{CM} = 0V, R_F = 1k\Omega, R_G = 174\Omega, \) both inputs terminated in 50\( \Omega \), \( R_L = 100\Omega \), Typical values, results referred to device output:

### Small Signal Frequency Response (\( A_V = 2 \))

![Small Signal Frequency Response Graph](image1)

### Large Signal Frequency Response (\( A_V = 2 \))

![Large Signal Frequency Response Graph](image2)

### Frequency Response over Temperature (\( A_V = 10 \))

![Frequency Response over Temperature Graph](image3)

### Frequency Response for Various \( V_G \) (\( A_{V\_MAX} = 10 \)) (\( \pm 2.5V \))

![Frequency Response for Various \( V_G \) Graph](image4)

### Frequency Response for Various \( V_G \) (\( A_{V\_MAX} = 10 \))

![Frequency Response for Various \( V_G \) Graph](image5)

### Small Signal Frequency Response

![Small Signal Frequency Response Graph for Different \( V_G \) Values](image6)
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{G,MAX}$, $V_{CM} = 0V$, $R_T = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$, Typical values, results referred to device output: (Continued)

Large Signal Frequency Response

Frequency Response for Various $V_G$ ($A_{VMAX} = 100$) (Small Signal)

Frequency Response for Various $V_G$ ($A_{VMAX} = 100$) (Large Signal)

Gain Control Frequency Response

$I_S$ vs. $V_S$

$I_S$ vs. $V_S$

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Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, 25°C, $V_G = V_{G\_MAX}$, $V_{CM} = 0V$, $R_F = 1\,k\Omega$, $R_G = 174\,\Omega$, both inputs terminated in 50Ω, $R_L = 100\,\Omega$, Typical values, results referred to device output: (Continued)
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{G,\text{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$, Typical values, results referred to device output.

(Continued)

**$A_{VMAX}$ vs. $V_{CM}$**

$V_S = \pm 2.5V$

$V_{IN,\text{DIFF}} = 0.1V$

$V_G = V_{G,\text{MAX}}$

**$A_{VMAX}$ vs. $V_{CM}$**

$V_S = \pm 5V$

$V_{IN,\text{DIFF}} = 0.1V$

$V_G = V_{G,\text{MAX}}$

**Supply Current vs. $V_{CM}$**

$V_S = \pm 5V$

$V_G = V_{G,\text{MAX}}$

**Supply Current vs. $V_{CM}$**

**Output Offset Voltage vs. $V_{CM}$ (Typical Unit 1)**

$V_S = \pm 5V$

$V_G = V_{G,\text{MAX}}$

**Output Offset Voltage vs. $V_{CM}$ (Typical Unit 2)**

$V_S = \pm 5V$

$V_G = V_{G,\text{MAX}}$
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_{G} = V_{G\_{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$, Typical values, results referred to device output: (Continued)

Output Offset Voltage vs. $V_{CM}$ (Typical Unit 3)

Gain Flatness and Linear Phase Deviation

Group Delay vs. Frequency

K Factor vs. $R_G$
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5\,\text{V}$, $25^\circ\text{C}$, $V_{G} = V_{G\_\text{MAX}}$, $V_{CM} = 0\,\text{V}$, $R_F = 1\,\text{k}\Omega$, $R_G = 174\,\text{Ω}$, both inputs terminated in $50\,\text{Ω}$, $R_L = 100\,\text{Ω}$, Typical values, results referred to device output: (Continued)
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{G,\text{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$, Typical values, results referred to device output: (Continued)
Typical Performance Characteristics

Unless otherwise specified: $V_G = \pm 5V$, 25°C, $V_G = V_{G\_MAX}$, $V_{CM} = 0V$, $R_F = 1\, k\Omega$, $R_G = 174\, \Omega$, both inputs terminated in 50Ω, $R_L = 100\, \Omega$, Typical values, results referred to device output: (Continued)

- Noise vs. Frequency ($A_{V\_MAX} = 100$)
- Output Voltage vs. Output Current
- $\pm 1\, db$ Compression
- HD2 vs. $P_{OUT}$
- HD3 vs. $P_{OUT}$
- THD vs. $P_{OUT}$
Typical Performance Characteristics

Unless otherwise specified: $V_S = \pm 5V$, 25˚C, $V_G = V_{G\_\text{MAX}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in 50Ω, $R_L = 100\Omega$, Typical values, results referred to device output: (Continued)
**Typical Performance Characteristics** Unless otherwise specified: $V_S = \pm 5V$, $25^\circ C$, $V_G = V_{G_{\text{MAX}}}$, $V_{CM} = 0V$, $R_F = 1k\Omega$, $R_G = 174\Omega$, both inputs terminated in $50\Omega$, $R_L = 100\Omega$, Typical values, results referred to device output: (Continued)

![Image](image1.png)

**Application Information**

**THEORY OF OPERATION**

The LMH6503 is a linear wideband variable-gain amplifier as illustrated in Figure 1. A voltage input signal may be applied differentially between the two inputs (+$V_{IN}$, $-V_{IN}$), or single-endedly by grounding one of the two unused inputs. The LMH6503 input buffers convert the input voltage to a current ($I_{RG}$) that is a function of the differential input voltage ($V_{INPUT} = (+V_{IN}) - (-V_{IN})$) and the value of the gain setting resistor ($RG$). This current ($I_{RG}$) is then mirrored to a gain stage with a current gain of $K$ (1.72 nominal). The voltage controlled two-quadrant multiplier attenuates this current which is then converted to a voltage via the output amplifier. This output amplifier is a current feedback op amp configured as a Transimpedance amplifier. Its Transimpedance gain is the feedback resistor ($RF$). The input signal, output, and gain control are all voltages. The output voltage can easily be calculated as shown in Equation 1:

$$V_{OUT} = I_{RG} \times K \times \frac{V_G + 1}{2} \times R_F \quad \text{FOR } -1 < V_G < +1$$

Where $K = 1.72$ (Nominal)

since:

$$I_{RG} = \frac{V_{INPUT}}{RG}$$

The gain of the LMH6503 is therefore a function of three external variables: $RG$, $RF$, and $V_G$ as expressed in Equation 2:

$$A_V = \frac{R_F}{R_G} \times 1.72 \times \frac{V_G + 1}{2}$$

The gain control voltage ($V_G$) has an ideal input range of $-1V < V_G < +1V$. At $V_G = +1V$, the gain of the LMH6503 is at its maximum as expressed in Equation 3:

$$A_V = \frac{R_F}{R_G}$$

Notice also that Equation 3 holds for both differential and single ended operation.

![Image](image2.png)

**CHOOSING $RF$ AND $RG$**

$RG$ is calculated from Equation 4. $V_{INPUTMAX}$ is the maximum peak input voltage ($V_{IN}$) determined by the application. $I_{RGMAX}$ is the maximum allowable current through $RG$ and is typically 2.3mA. Once $A_{VMAX}$ is determined from the minimum input and desired output voltages, $RF$ is then determined using Equation 5. These values of $RF$ and $RG$ are

![Image](image3.png)
Application Information

(Continued)

The minimum possible values that meet the input voltage and maximum gain constraints. Scaling the resistor values will decrease bandwidth and improve stability.

Figure 2 illustrates the resulting LMH6503 bandwidths as a function of the maximum (y axis) and minimum (related to x axis) input voltages when V_OUT is held constant at 1V_pp.

GAIN ACCURACY

Defined as the ratio of measured gain (V/V), at a certain V_G, to the best fit line drawn through the typical gain (V/V) distribution for −1V < V_G < 1V (results expressed in dB) (See Figure 4). The best fit gain (A_V) is given by:

\[
A_V (V/V) = 4.87V_G + 4.61 \tag{6}
\]

For: −1V ≤ V_G ≤ +1V, R_F = 1kΩ, R_G = 174Ω

For a V_G range, the value specified in the tables represents the worst case accuracy over the entire range. The "Typical" value would be the worst case ratio between the "Typical Gain" and the best fit line. The "Max" value would be the worst case between the max/min gain limit and the best fit line.

GAIN MATCHING

Defined as the limit on gain variation at a certain V_G (expressed in dB) (See Figure 4). Specified as "Max" only. For a V_G range, the value specified represents the worst case matching over the entire range. The "Max" value would be the worst case ratio between the max/min gain limit and the typical gain.

FIGURE 2. Bandwidth vs. V_INMAX and A_VMAX

FIGURE 3. Nulling the Output Offset Voltage

FIGURE 4. Gain Accuracy and Gain Matching

Parameters Defined
Application Information (Continued)

NOISE

Figure 5 describes the LMH6503’s output-referred spot noise density as a function of frequency with \( AV_{\text{MAX}} = 10 \text{V/V} \). The plot includes all the noise contributing terms. However, with both inputs terminated in 50\( \Omega \), the input noise contribution is minimal. At \( AV_{\text{MAX}} = 10 \text{V/V} \), the LMH6503 has a typical flat-band input-referred spot noise density \( e_{\text{in}} \) of 6.6nV/\( \sqrt{\text{Hz}} \). For applications with −3dB BW extending well into the flat-band region, the input RMS voltage noise can be determined from the following single-pole model:

\[
V_{\text{RMS}} = e_{\text{in}} \sqrt{1.57 \times (-3\text{dB BANDWIDTH})}
\]

\( V_{\text{RMS}} \) is the RMS voltage noise at the output, \( e_{\text{in}} \) is the input-referred voltage noise, and the \(-3\text{dB BANDWIDTH}\) is the bandwidth at which the gain is halved from the maximum gain.

![Figure 5](image-url)  
**FIGURE 5. Output Referred Voltage Noise vs. Frequency**

CIRCUIT LAYOUT CONSIDERATIONS

Good high-frequency operation requires all of the decoupling capacitors shown in Figure 6 to be placed as close as possible to the power supply pins in order to insure a proper high-frequency low-impedance bypass. Adequate ground plane and low inductive power returns are also required of the layout. Minimizing the parasitic capacitances at pins 3, 4, 5, 6, 9, 10 and 12 will assure best high frequency performance. The parasitic inductance of component leads or traces to pins 4, 5 and 9 should also be kept to a minimum. Parasitic or load capacitance, \( C_L \), on the output (pin 10) degrades phase margin and can lead to frequency response peaking or circuit oscillation. The LMH6503 is fully stable when driving a 100\( \Omega \) load. With reduced load (e.g. 1k\( \Omega \)) there is a possibility of instability at very high frequencies beyond 400MHz especially with a capacitive load. When the LMH6503 is connected to a light load as such, it is recommended to add a snubber network to the output (e.g. 100\( \Omega \) and 39pF in series tied between the LMH6503 output and ground). \( C_L \) can also be isolated from the output by placing a small resistor in series with the output (pin 10).

Component parasitics also influence high frequency results. Therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended.

National Semiconductor suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization:

<table>
<thead>
<tr>
<th>Device Package</th>
<th>Evaluation Board Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6503MA SOIC-14</td>
<td>CLC730033</td>
</tr>
<tr>
<td>LMH6503MT TSSOP-14</td>
<td>CLC730146</td>
</tr>
</tbody>
</table>

The evaluation board is shipped when a device sample request is placed with National Semiconductor.

SINGLE SUPPLY OPERATION

It is possible to operate the LMH6503 with a single supply. To do so, tie pin 11 (GND) to a potential about mid point between \( V^+ \) and \( V^- \). Two examples are shown in Figure 7 & Figure 8.

![Figure 7](image-url)  
**FIGURE 7. AC Coupled Single Supply VGA**
OPERATING AT LOWER SUPPLY VOLTAGES

The LMH6503 is rated for operation down to 5V supplies (V+ - V−). There are some specifications shown for operation at ±2.5V within the data sheet (i.e. Frequency Response, CMRR, PSRR, Gain vs. VG, etc.). Compared to ±5V operation, at lower supplies:

a) VG range constricts. Referring to Figure 9, note that VG_MAX (VG voltage required to get maximum gain) is 0.5V (VS = ±2.5V) compared to 1.0V for VS = ±5V. At the same time, gain cut-off (VG_MIN) would shift to −0.5V from −1V with VS = ±5V.

Table 1 shows the approximate expressions for various VG voltages as a function of V−:

<table>
<thead>
<tr>
<th>VG</th>
<th>Definition</th>
<th>Expression (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VG_MIN</td>
<td>Gain Cut-off</td>
<td>0.2 x V−</td>
</tr>
<tr>
<td>VG_MID</td>
<td>AVMAX/2</td>
<td>0</td>
</tr>
<tr>
<td>VG_MAX</td>
<td>AVMAX</td>
<td>−0.2 x V−</td>
</tr>
</tbody>
</table>

b) VG_LIMIT (maximum permissible voltage on VG) is reduced. This is due to limitations within the device arising from transistor headroom. Beyond this limit, device performance will be affected (non-destructive). Referring to Figure 9, note that with V+ = 2.5V, and V− = −4V, VG_LIMIT is approaching VG_MAX and already “Max gain” is reduced by 1dB. This means that operating under these conditions has reduced the maximum permissible voltage on VG to a level below what is needed to get Max gain. If supply voltages are asymmetrical, reference Figure 9 and Figure 10 plots to make sure the region of operation is not overly restricted by the “pinching” of VG LIMIT and VG MAX CURVES.

c) “Max_gain” reduces. There is an intrinsic reduction in max gain when the total supply voltage is reduced (see Typical Performance Characteristics plots for Gain vs. VG (VS = ±2.5V). In addition, there is the more drastic mechanism described in “b” above and shown in Figure 9.

Similar plots for V+ = 5V operation are shown in Figure 10 for comparison and reference.
Application Circuits

FOUR-QUADRANT MULTIPLIER
Applications requiring multiplication, squaring or other non-linear functions can be implemented with four-quadrant multipliers. The LMH6503 implements a four-quadrant multiplier as illustrated in Figure 11:

FREQUENCY SHAPING
Frequency shaping and bandwidth extension of the LMH6503 can be accomplished using parallel networks connected across the RG ports. The network shown in the Figure 12 schematic will effectively extend the LMH6503’s bandwidth.

2nd ORDER TUNABLE BANDPASS FILTER
The LMH6503 Variable-Gain Amplifier placed into a feedback loop provides signal processing function such as in a 2nd order tunable bandpass filter. The center frequency of the 2nd order bandpass shown in Figure 13 is adjusted through the use of the LMH6503’s gain control voltage, V_G. The integrators implemented with two sections of a LMH6682, provide the coefficients for the transfer function.
Physical Dimensions inches (millimeters) unless otherwise noted

14-Pin SOIC
NS Package Number M14A

14-Pin TSSOP
NS Package Number MTC14
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