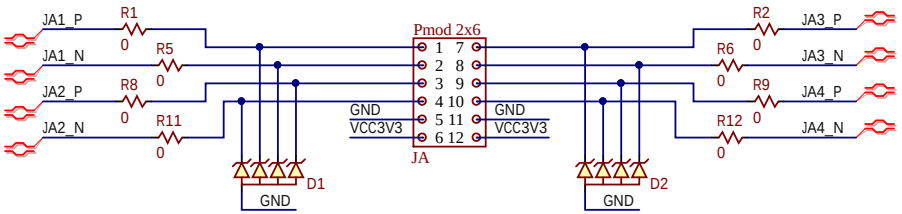


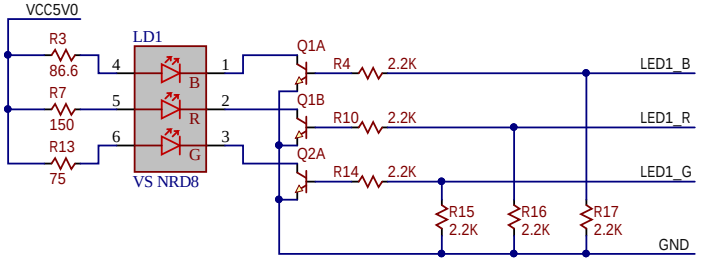


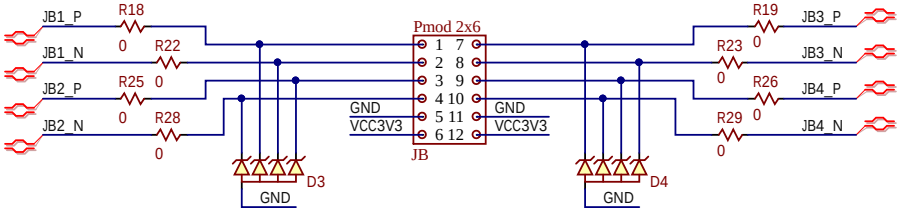


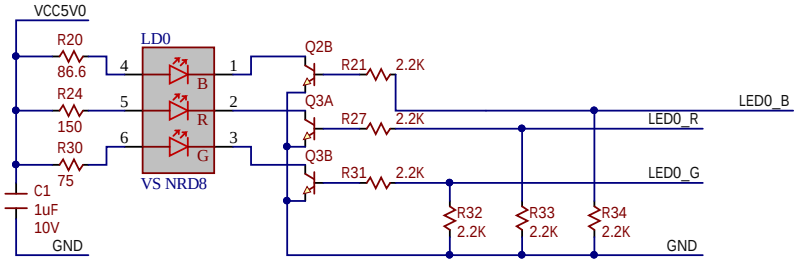


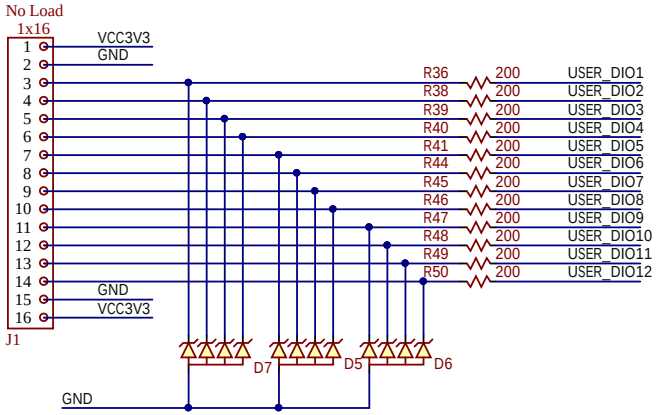


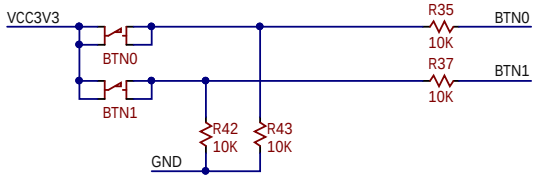


Foot F1
Foot F2
Foot F3
Foot F4

Digilent Inc. CE ROHS Chinese ROHS Cora Z7

| | |
|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | PMODs, User I/O |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 1 out of 11 |

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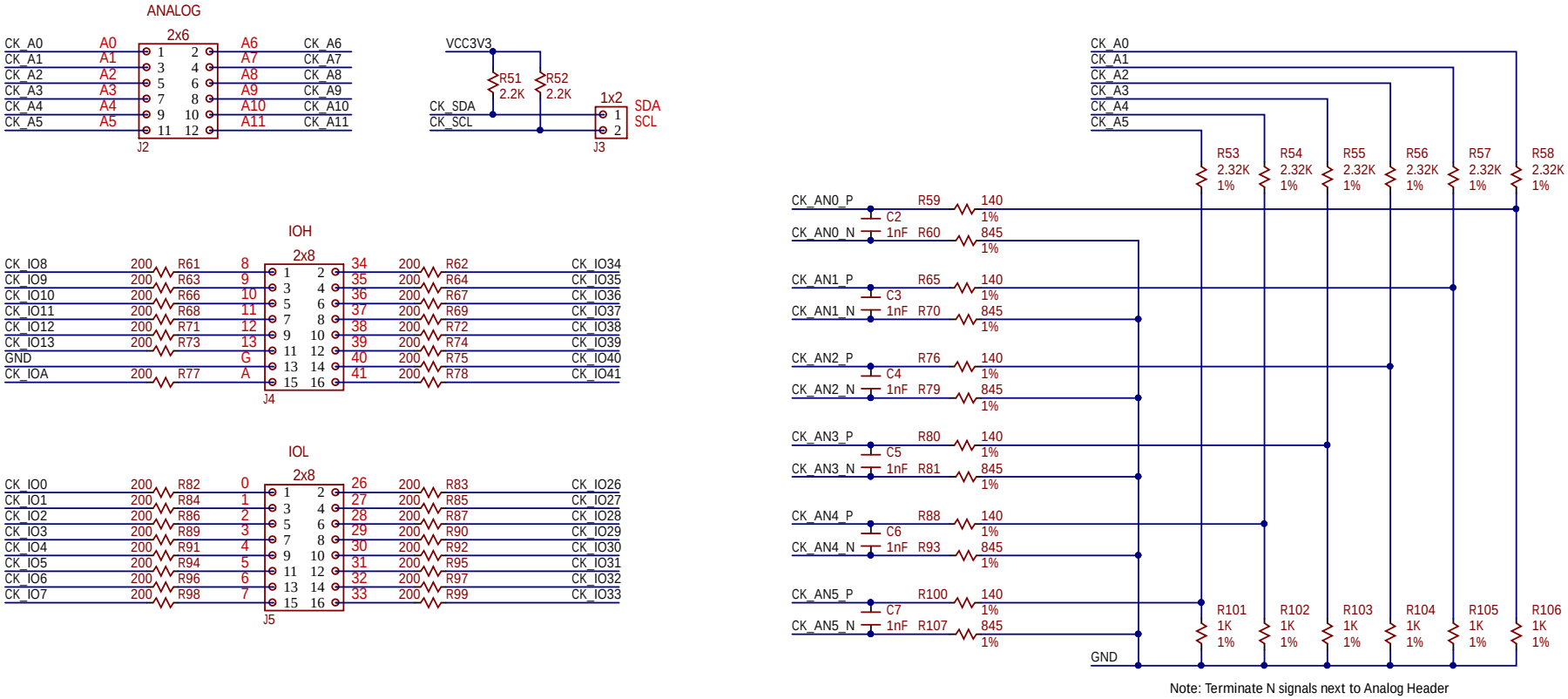


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|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | CHipKIT IO |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 2 out of 11 |

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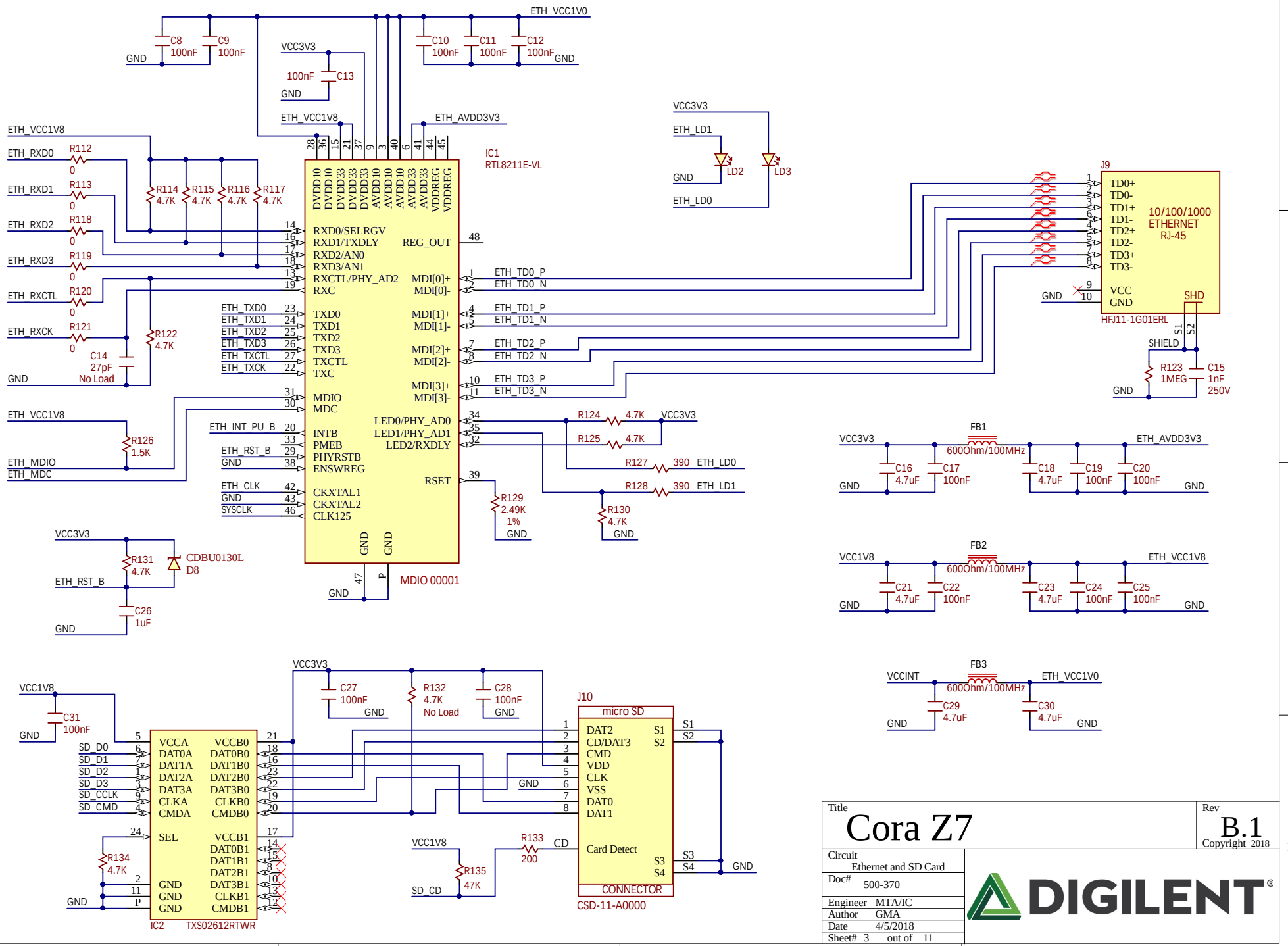
ETH_VCC1V0
C8 100nF
C9 100nF
C10 100nF
C11 100nF
C12 100nF
GND
VCC3V3
C13 100nF
ETH_VCC1V8
ETH_AVDD3V3
IC1
RTL8211E-VL
DVDD10
DVDD10
DVDD33
DVDD33
AVDD10
AVDD10
AVDD33
AVDD33
VDDREG
VDDREG
RXD0/SELRGV
RXD1/TXDLY
RXD2/AN0
RXD3/AN1
RXCTL/PHY_AD2
RXC
REG_OUT
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
TXD0
TXD1
TXD2
TXD3
TXCTL
TXC
MDIO
MDC
LED0/PHY_AD0
LED1/PHY_AD1
LED2/RXDLY
INTB
PMEB
PHYRSTB
ENSWREG
RSET
CKXTAL1
CKXTAL2
CLK125
SYSCLK
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXCTL
ETH_RXCK
R112 0
R113 0
R118 0
R119 0
R120 0
R121 0
R114 4.7K
R115 4.7K
R116 4.7K
R117 4.7K
R122 4.7K
C14 27pF No Load
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXCTL
ETH_TXCK
ETH_TD0_P
ETH_TD0_N
ETH_TD1_P
ETH_TD1_N
ETH_TD2_P
ETH_TD2_N
ETH_TD3_P
ETH_TD3_N
ETH_INT_PU_B
ETH_RST_B
ETH_CLK
ETH_MDIO
ETH_MDC
R126 1.5K
R124 4.7K
R125 4.7K
R127 390
R128 390
ETH_LD0
ETH_LD1
R129 2.49K 1%
R130 4.7K
MDIO 00001
VCC3V3
ETH_LD1
LD2
LD3
GND
ETH_LD0
J9
TD0+
TD0-
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
VCC
GND
SHD
10/100/1000 ETHERNET RJ-45
HFJ11-1G01ERL
SHIELD
S1
S2
R123 1MEG
C15 1nF 250V
FB1
600Ohm/100MHz
C16 4.7uF
C17 100nF
C18 4.7uF
C19 100nF
C20 100nF
FB2
C21 4.7uF
C22 100nF
C23 4.7uF
C24 100nF
C25 100nF
FB3
VCCINT
C29 4.7uF
C30 4.7uF
R131 4.7K
CDBU0130L
D8
C26 1uF
VCC1V8
C31 100nF
C27 100nF
R132 4.7K No Load
C28 100nF
J10
micro SD
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
Card Detect
CONNECTOR
CSD-11-A0000
SD_D0
SD_D1
SD_D2
SD_D3
SD_CCLK
SD_CMD
VCCA
DAT0A
DAT1A
DAT2A
DAT3A
CLKA
CMDA
VCCB0
DAT0B0
DAT1B0
DAT2B0
DAT3B0
CLKB0
CMDB0
SEL
VCCB1
DAT0B1
DAT1B1
DAT2B1
DAT3B1
CLKB1
CMDB1
IC2
TXS02612RTWR
R134 4.7K
R133 200
R135 47K
CD
SD_CD
Title
Cora Z7
Rev
B.1
Copyright 2018
Circuit
Ethernet and SD Card
Doc#
500-370
Engineer MTA/IC
Author GMA
Date 4/5/2018
Sheet# 3 out of 11
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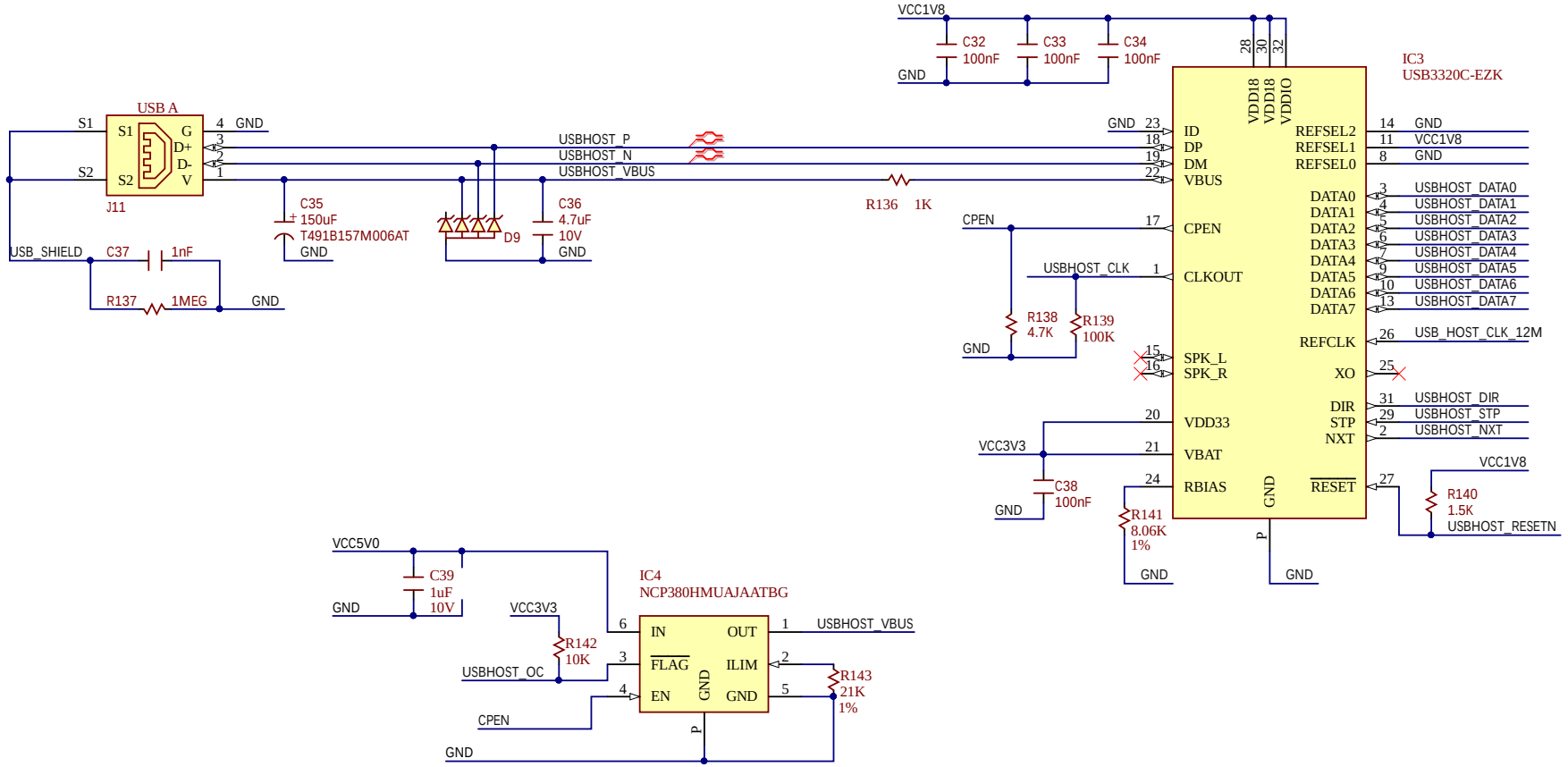


| | |
|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | USB HOST |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 4 out of 11 |

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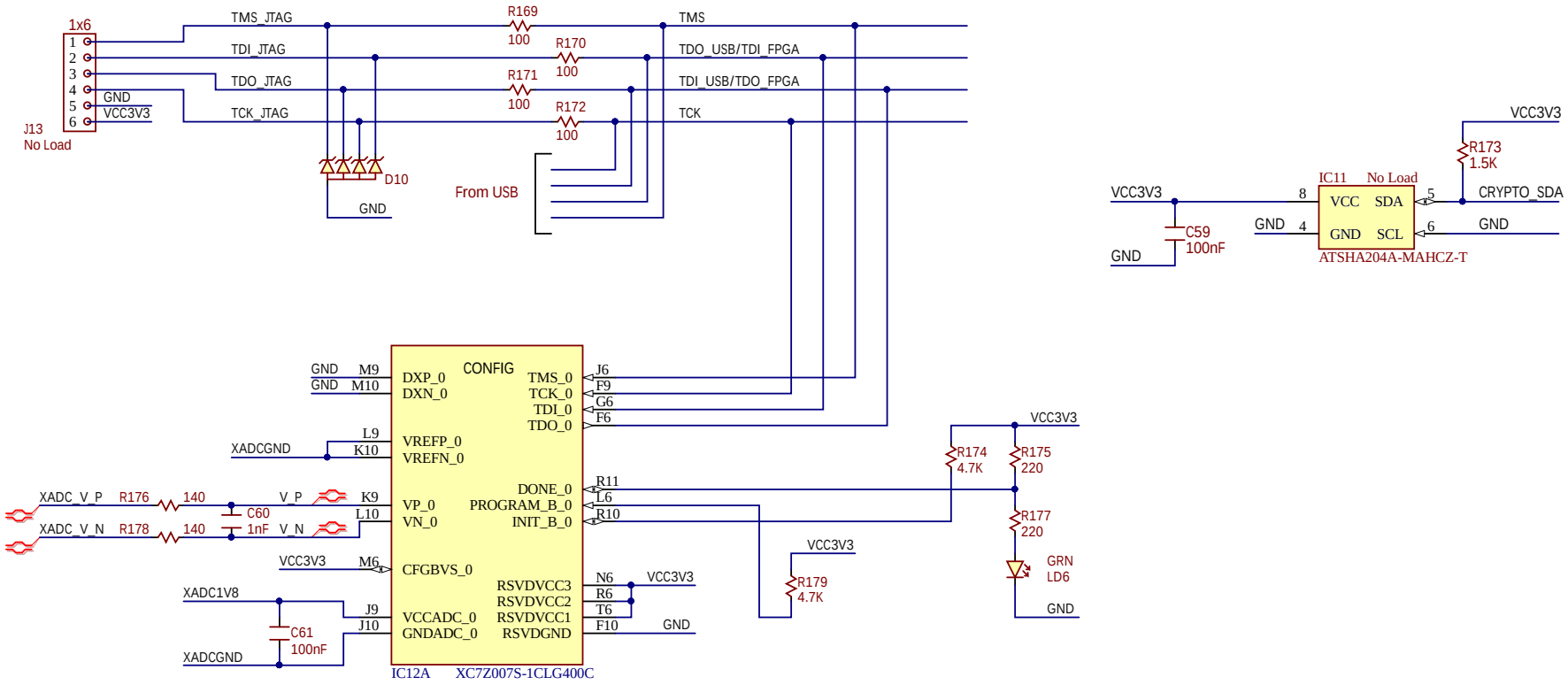


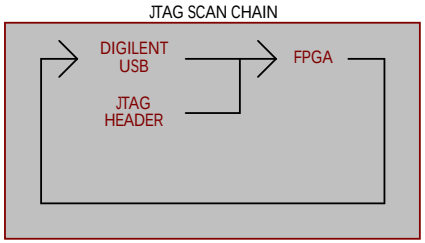


| | |
|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | FPGA Configuration |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 6 out of 11 |

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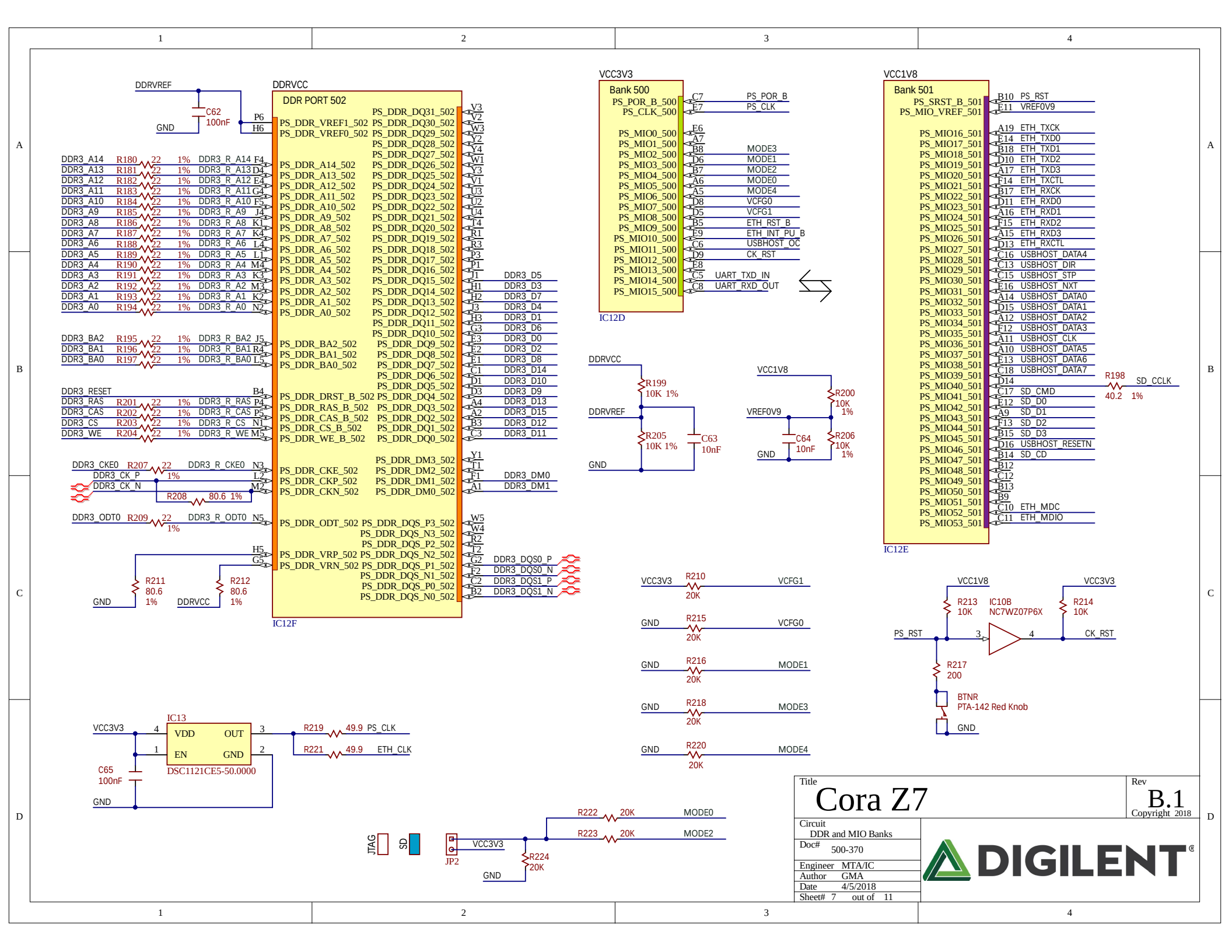
DDRVREF
DDRVCC
DDR PORT 502
C62
100nF
GND
P6
H6
IC12F
VCC3V3
Bank 500
IC12D
PS_POR_B_500
PS_CLK_500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
PS_POR_B
PS_CLK
MODE3
MODE1
MODE2
MODE0
MODE4
VCFG0
VCFG1
ETH_RST_B
ETH_INT_PU_B
USBHOST_OC
CK_RST
UART_TXD_IN
UART_RXD_OUT
VCC1V8
Bank 501
IC12E
PS_SRST_B_501
PS_MIO_VREF_501
PS_RST
VREF0V9
ETH_TXCK
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXCTL
ETH_RXCK
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXCTL
USBHOST_DATA4
USBHOST_DIR
USBHOST_STP
USBHOST_NXT
USBHOST_DATA0
USBHOST_DATA1
USBHOST_DATA2
USBHOST_DATA3
USBHOST_CLK
USBHOST_DATA5
USBHOST_DATA6
USBHOST_DATA7
SD_CCLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
USBHOST_RESETN
SD_CD
ETH_MDC
ETH_MDIO
R198
40.2 1%
DDR3_A14 R180 22 1% DDR3_R_A14
DDR3_A13 R181 22 1% DDR3_R_A13
DDR3_A12 R182 22 1% DDR3_R_A12
DDR3_A11 R183 22 1% DDR3_R_A11
DDR3_A10 R184 22 1% DDR3_R_A10
DDR3_A9 R185 22 1% DDR3_R_A9
DDR3_A8 R186 22 1% DDR3_R_A8
DDR3_A7 R187 22 1% DDR3_R_A7
DDR3_A6 R188 22 1% DDR3_R_A6
DDR3_A5 R189 22 1% DDR3_R_A5
DDR3_A4 R190 22 1% DDR3_R_A4
DDR3_A3 R191 22 1% DDR3_R_A3
DDR3_A2 R192 22 1% DDR3_R_A2
DDR3_A1 R193 22 1% DDR3_R_A1
DDR3_A0 R194 22 1% DDR3_R_A0
DDR3_BA2 R195 22 1% DDR3_R_BA2
DDR3_BA1 R196 22 1% DDR3_R_BA1
DDR3_BA0 R197 22 1% DDR3_R_BA0
DDR3_RESET
DDR3_RAS R201 22 1% DDR3_R_RAS
DDR3_CAS R202 22 1% DDR3_R_CAS
DDR3_CS R203 22 1% DDR3_R_CS
DDR3_WE R204 22 1% DDR3_R_WE
DDR3_CKE0 R207 22 1% DDR3_R_CKE0
DDR3_CK_P
DDR3_CK_N
R208 80.6 1%
DDR3_ODT0 R209 22 1% DDR3_R_ODT0
R211 80.6 1%
R212 80.6 1%
PS_DDR_VREF1_502
PS_DDR_VREF0_502
PS_DDR_A14_502
PS_DDR_A13_502
PS_DDR_A12_502
PS_DDR_A11_502
PS_DDR_A10_502
PS_DDR_A9_502
PS_DDR_A8_502
PS_DDR_A7_502
PS_DDR_A6_502
PS_DDR_A5_502
PS_DDR_A4_502
PS_DDR_A3_502
PS_DDR_A2_502
PS_DDR_A1_502
PS_DDR_A0_502
PS_DDR_BA2_502
PS_DDR_BA1_502
PS_DDR_BA0_502
PS_DDR_DRST_B_502
PS_DDR_RAS_B_502
PS_DDR_CAS_B_502
PS_DDR_CS_B_502
PS_DDR_WE_B_502
PS_DDR_CKE_502
PS_DDR_CKP_502
PS_DDR_CKN_502
PS_DDR_ODT_502
PS_DDR_VRP_502
PS_DDR_VRN_502
PS_DDR_DQ31_502
PS_DDR_DQ30_502
PS_DDR_DQ29_502
PS_DDR_DQ28_502
PS_DDR_DQ27_502
PS_DDR_DQ26_502
PS_DDR_DQ25_502
PS_DDR_DQ24_502
PS_DDR_DQ23_502
PS_DDR_DQ22_502
PS_DDR_DQ21_502
PS_DDR_DQ20_502
PS_DDR_DQ19_502
PS_DDR_DQ18_502
PS_DDR_DQ17_502
PS_DDR_DQ16_502
PS_DDR_DQ15_502
PS_DDR_DQ14_502
PS_DDR_DQ13_502
PS_DDR_DQ12_502
PS_DDR_DQ11_502
PS_DDR_DQ10_502
PS_DDR_DQ9_502
PS_DDR_DQ8_502
PS_DDR_DQ7_502
PS_DDR_DQ6_502
PS_DDR_DQ5_502
PS_DDR_DQ4_502
PS_DDR_DQ3_502
PS_DDR_DQ2_502
PS_DDR_DQ1_502
PS_DDR_DQ0_502
PS_DDR_DM3_502
PS_DDR_DM2_502
PS_DDR_DM1_502
PS_DDR_DM0_502
PS_DDR_DQS_P3_502
PS_DDR_DQS_N3_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_P0_502
PS_DDR_DQS_N0_502
DDR3_D5
DDR3_D3
DDR3_D7
DDR3_D4
DDR3_D1
DDR3_D6
DDR3_D0
DDR3_D2
DDR3_D8
DDR3_D14
DDR3_D10
DDR3_D9
DDR3_D13
DDR3_D15
DDR3_D12
DDR3_D11
DDR3_DM0
DDR3_DM1
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
DDRVCC
R199 10K 1%
DDRVREF
R205 10K 1%
C63 10nF
GND
VCC1V8
R200 10K 1%
VREF0V9
C64 10nF
R206 10K 1%
GND
VCC3V3 R210 20K VCFG1
GND R215 20K VCFG0
GND R216 20K MODE1
GND R218 20K MODE3
GND R220 20K MODE4
VCC1V8
R213 10K
IC10B NC7WZ07P6X
R214 10K
VCC3V3
PS_RST
CK_RST
R217 200
BTNR PTA-142 Red Knob
GND
IC13
VCC3V3
VDD
OUT
EN
GND
DSC1121CE5-50.0000
C65 100nF
GND
R219 49.9 PS_CLK
R221 49.9 ETH_CLK
JTAG
SD
JP2
VCC3V3
R222 20K MODE0
R223 20K MODE2
R224 20K
GND
Title
Cora Z7
Rev
B.1
Copyright 2018
Circuit
DDR and MIO Banks
Doc#
500-370
Engineer MTA/IC
Author GMA
Date 4/5/2018
Sheet# 7 out of 11
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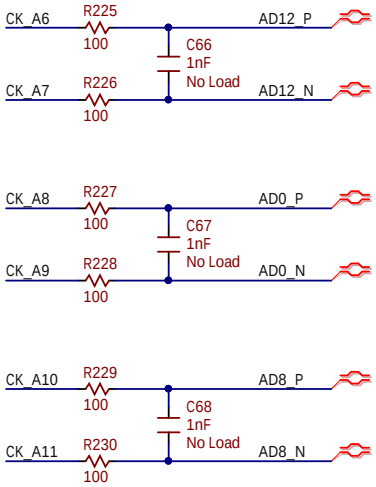


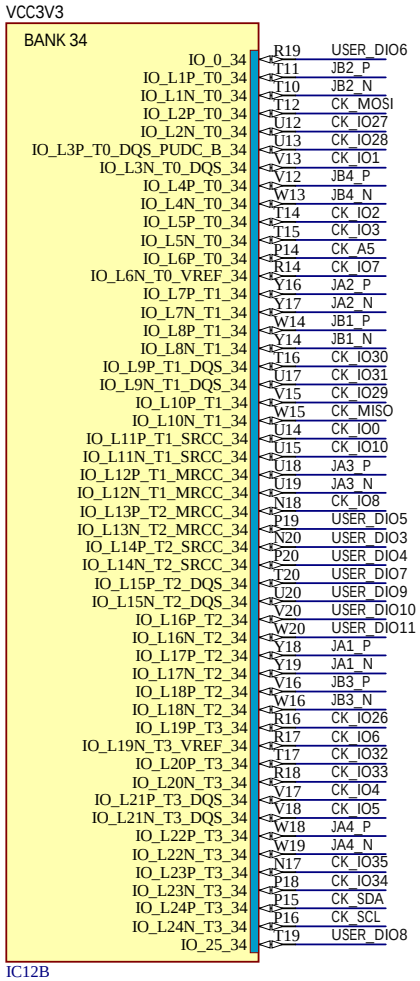


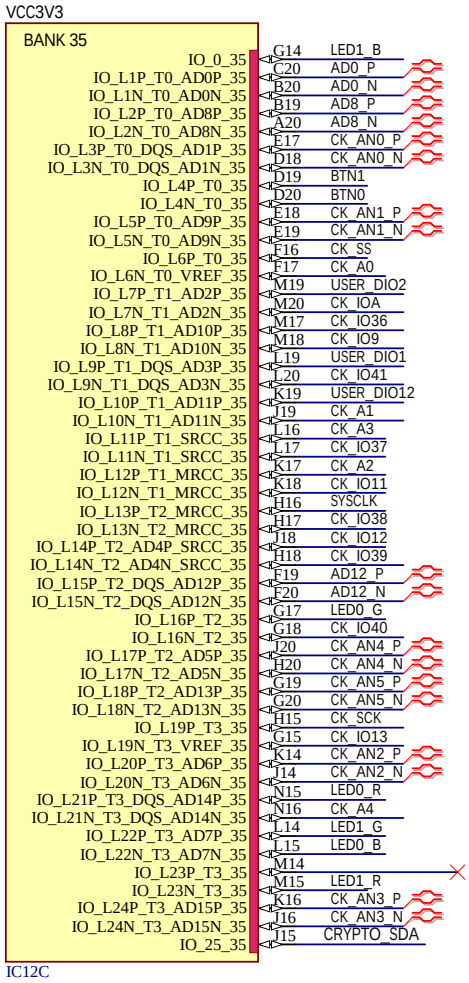


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|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | FPGA Banks, Anti Alias Filters |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 8 out of 11 |

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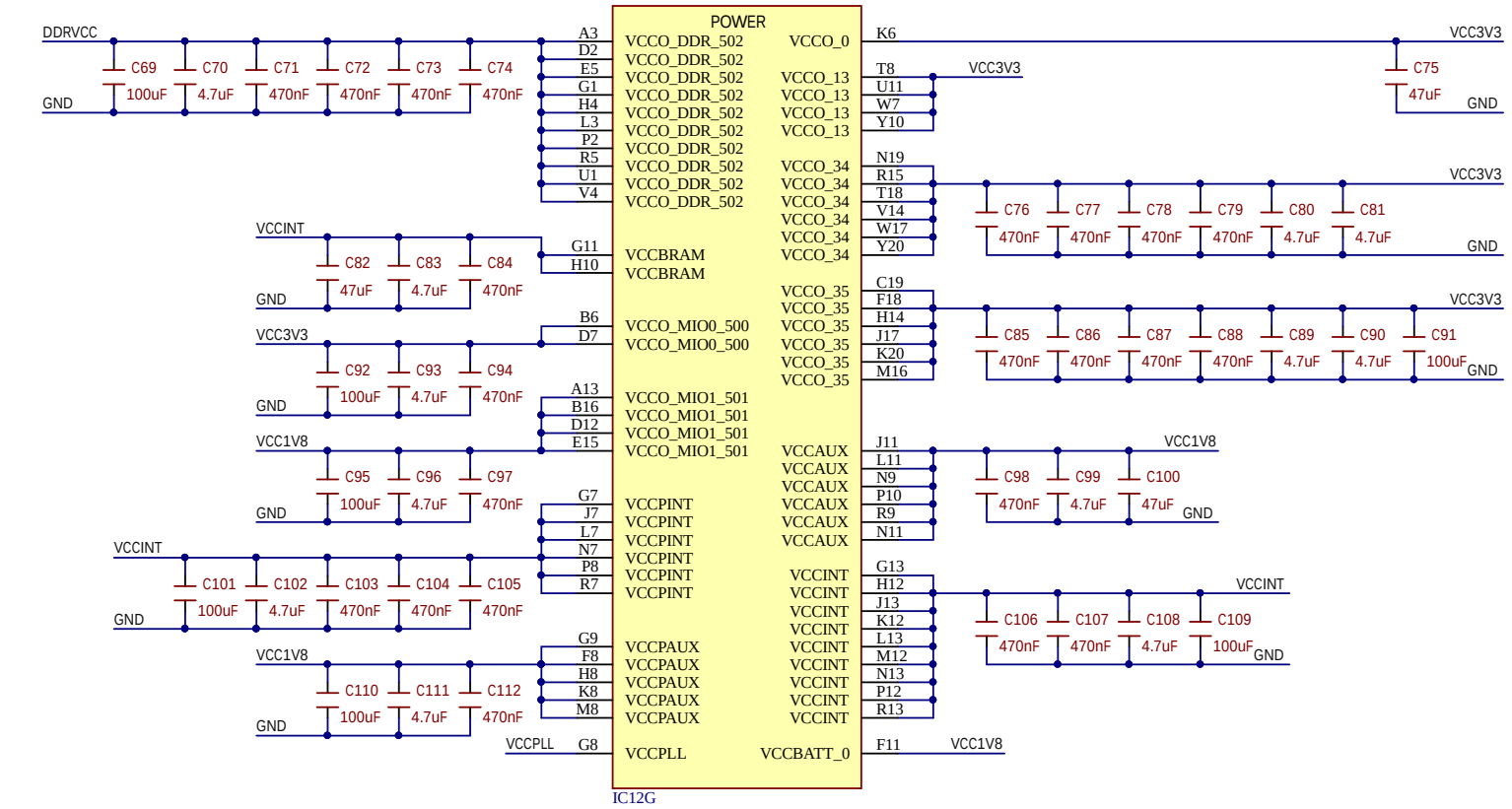


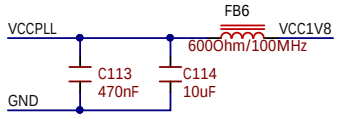


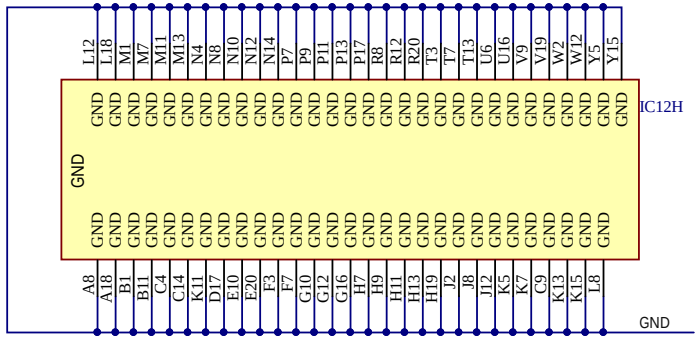


| | |
|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | FPGA Power |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 9 out of 11 |

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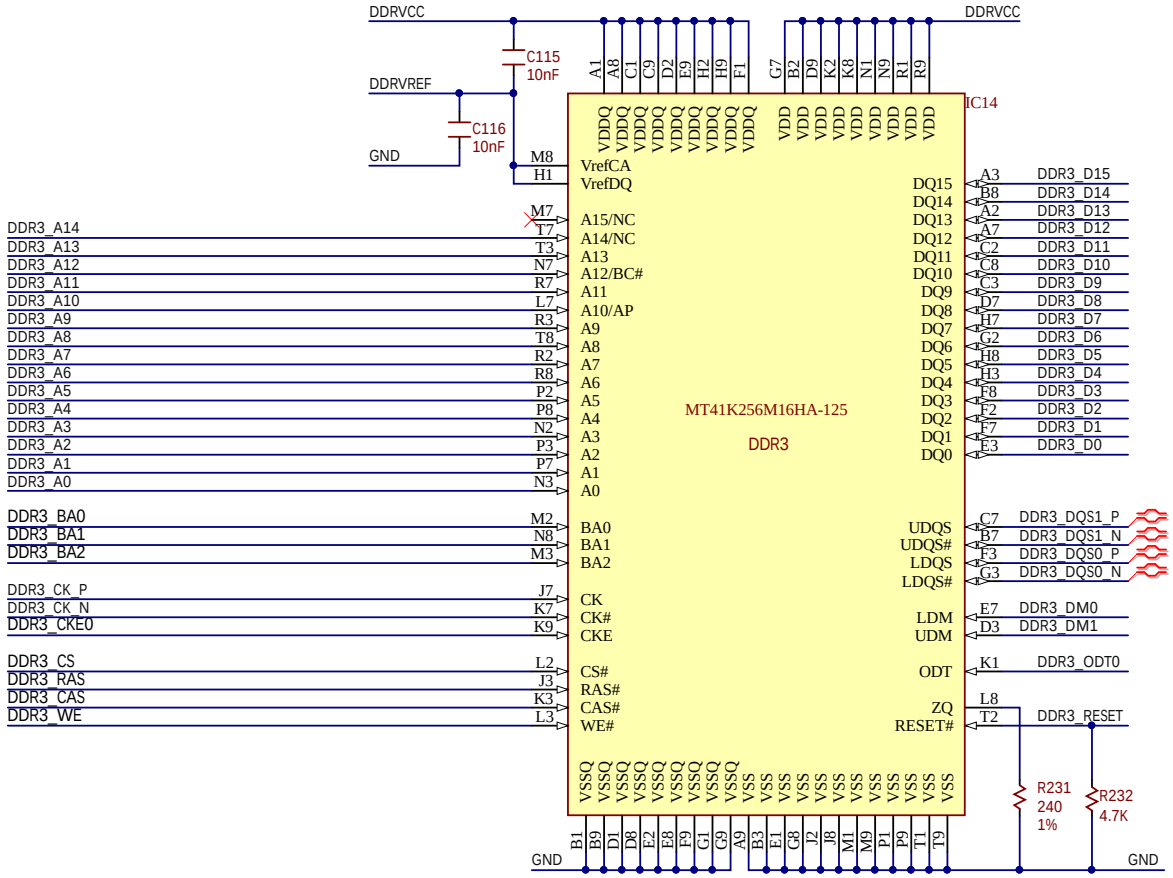


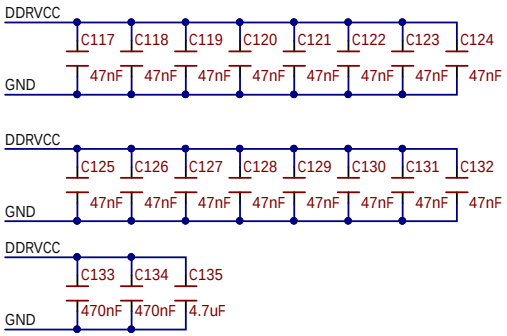


| | |
|---|---|
| Title | Cora Z7 |
| Rev | B.1 |
| Copyright | 2018 |
| Circuit | DDR3L Memory |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 10 out of 11 |

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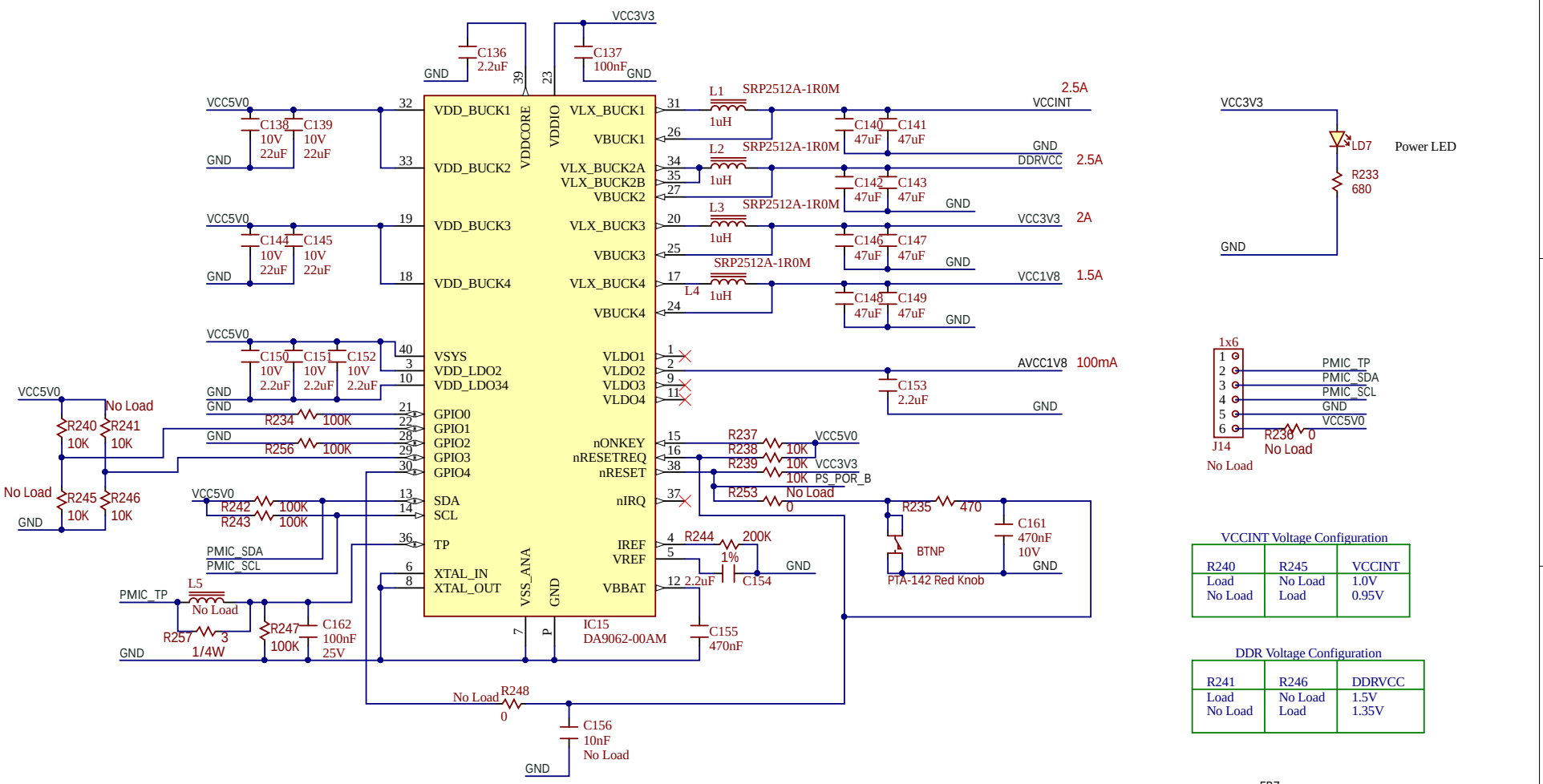









VCCINT Voltage Configuration

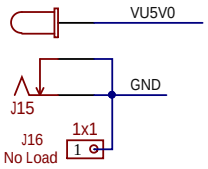
| R240 | R245 | VCCINT |
|---|---|---|
| Load | No Load | 1.0V |
| No Load | Load | 0.95V |

DDR Voltage Configuration

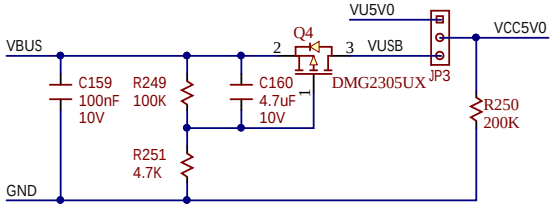
| R241 | R246 | DDRVCC |
|---|---|---|
| Load | No Load | 1.5V |
| No Load | Load | 1.35V |



Note: Input Voltage 5V only!




Power Select




| Title | Rev |
|---|---|
| Cora Z7 | B.1 |
| | Copyright 2018 |

| | |
|---|---|
| Circuit | Power Regulation |
| Doc# | 500-370 |
| Engineer | MTA/IC |
| Author | GMA |
| Date | 4/5/2018 |
| Sheet# | 11 out of 11 |

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