FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

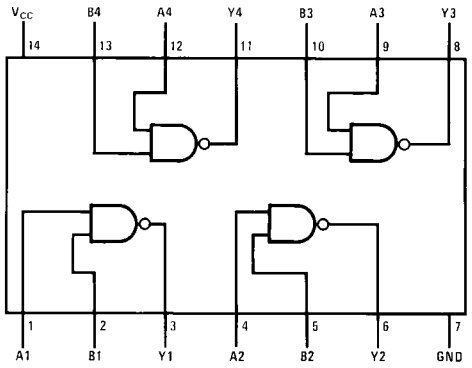
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

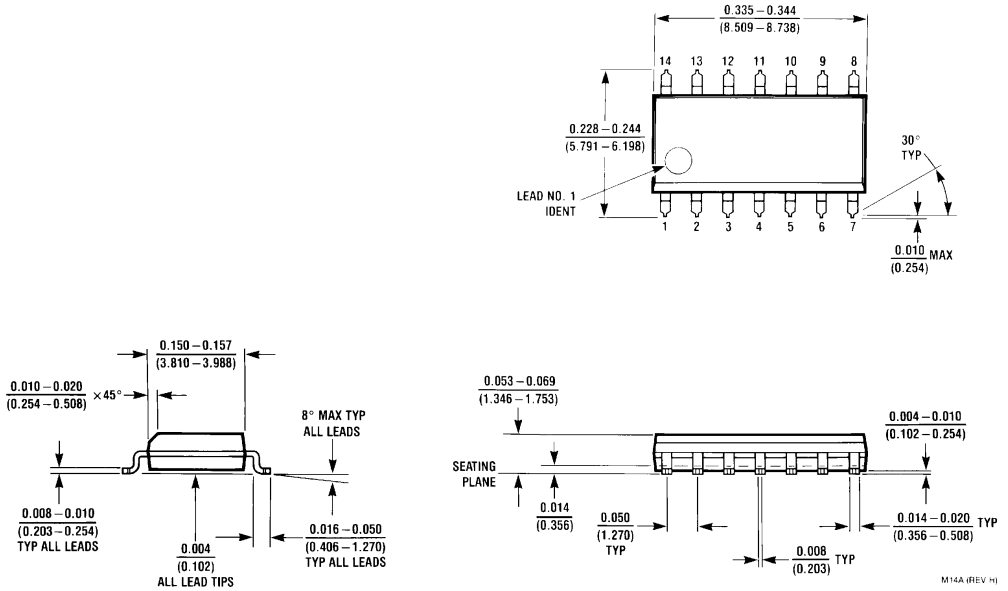
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

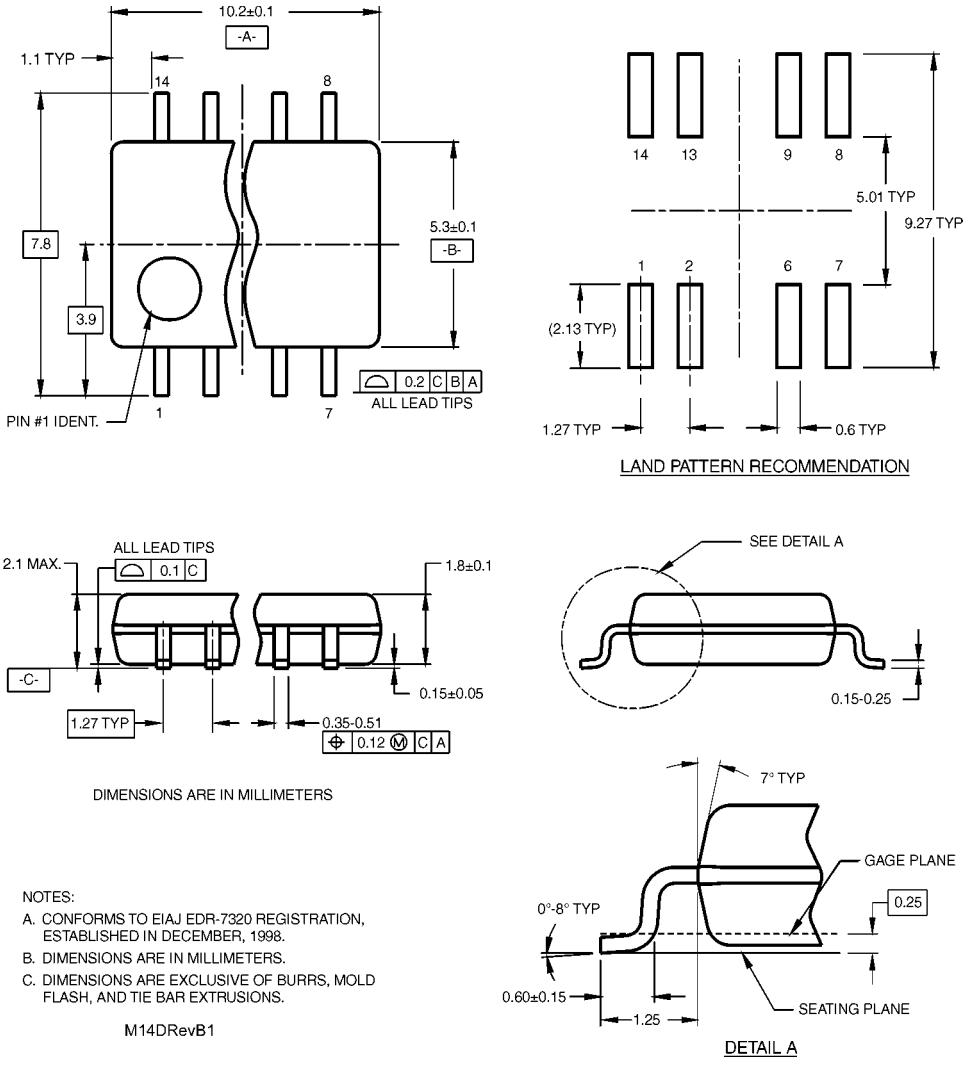
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

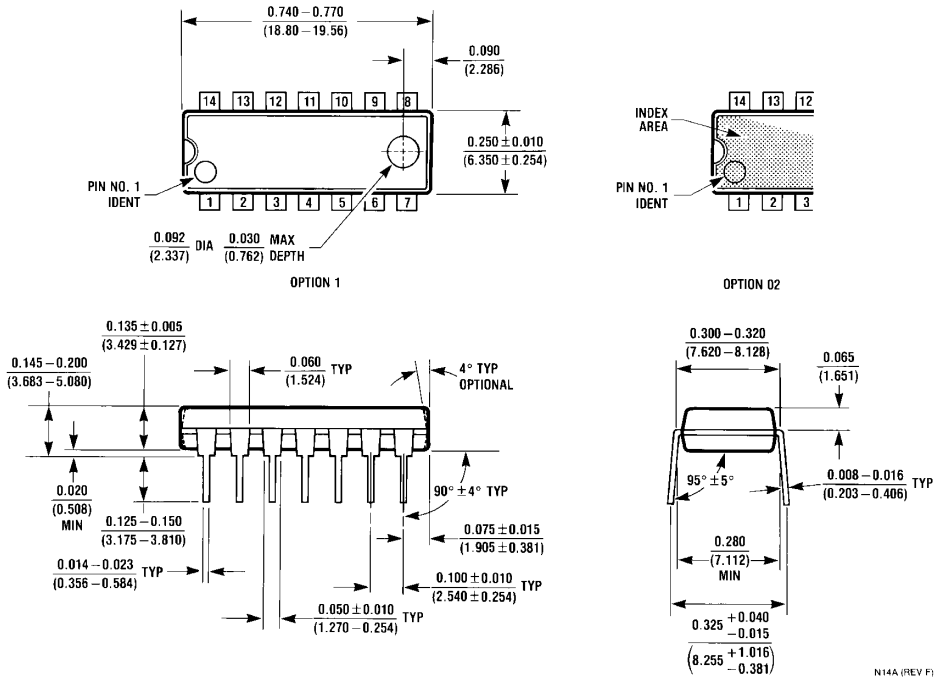
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM7404
Hex Inverting Gates

General Description

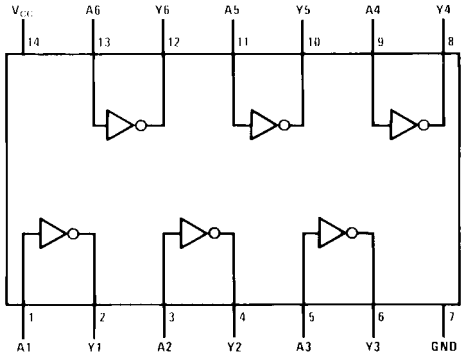
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{A}$$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		18	33	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

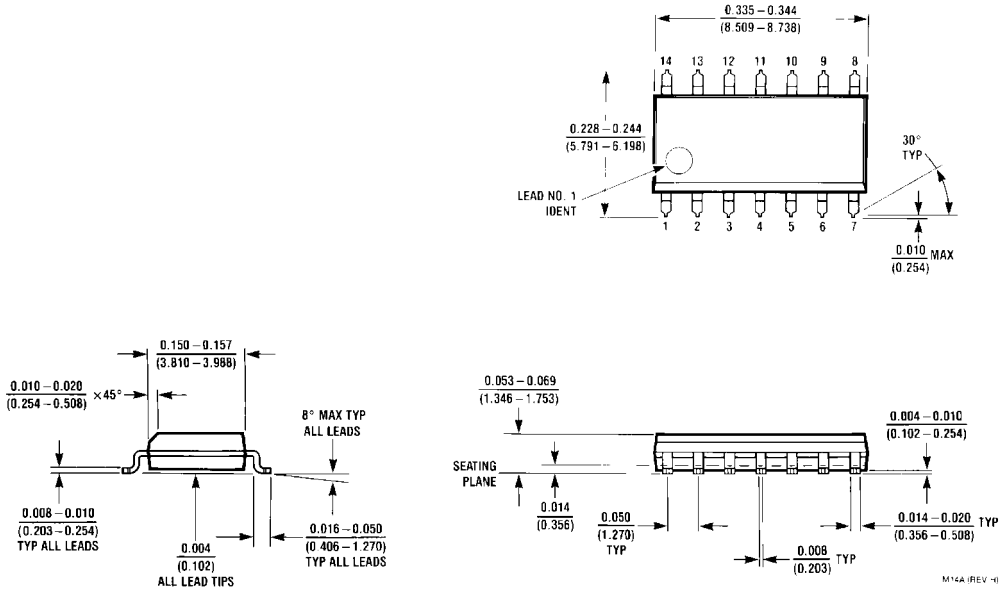
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

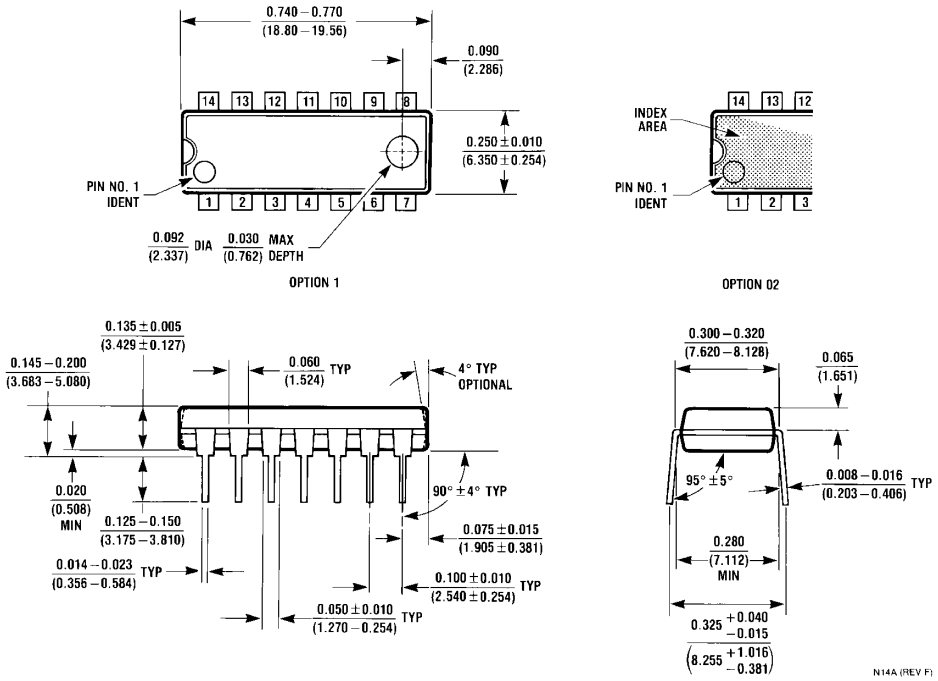
Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

FAIRCHILD SEMICONDUCTOR™

September 1986
Revised April 2000

DM74LS157 • DM74LS158
Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The DM74LS157 presents true data whereas the DM74LS158 presents inverted data to minimize propagation delay time.

Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Typical Propagation Time
  - DM74LS157 9 ns
  - DM74LS158 7 ns
- Typical Power Dissipation
  - DM74LS157 49 mW
  - DM74LS158 24 mW

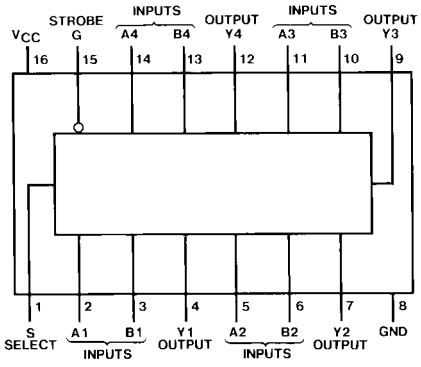
Ordering Code:

Order Number	Package Number	Package Description
DM74LS157M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS157SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS157N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS158M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS158N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

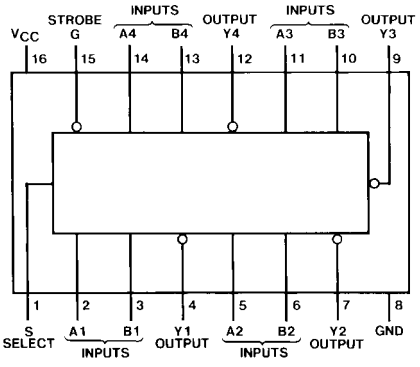
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

DM74LS157



DM74LS158



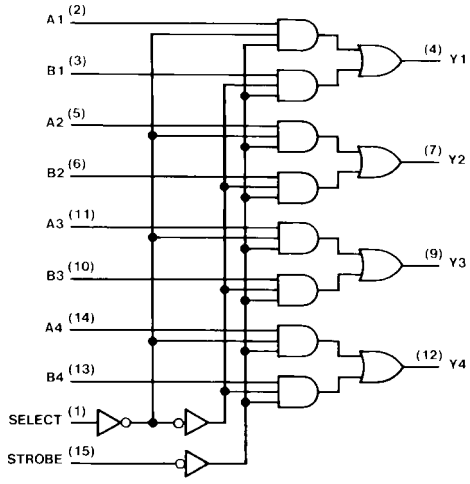
Function Table

Inputs				Output Y	
Strobe	Select	A	B	DM74LS157	DM74LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

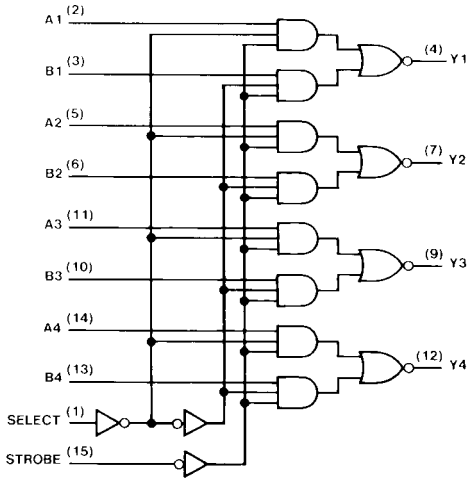
H = HIGH Level
L = LOW Level
X = Don't Care

Logic Diagrams

DM74LS157



DM74LS158



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS157 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS157 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	S or G			0.2	mA
		V_I = 7V	A or B			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = Max	S or G			40	µA
		V_I = 2.7V	A or B			20	
I_{IL}	LOW Level Input Current	V_{CC} = Max	S or G			−0.8	mA
		V_I = 0.4V	A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9.7	16	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with 4.5V applied to all inputs and all outputs OPEN.

DM74LS157 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Y		14		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Y		14		23	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Strobe to Y		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Strobe to Y		21		30	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Y		23		28	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Y		27		32	ns

DM74LS158 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS158 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	S or G A or B			0.2 0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.7V	S or G A or B			40 20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	S or G A or B			−0.8 −0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			4.8	8	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

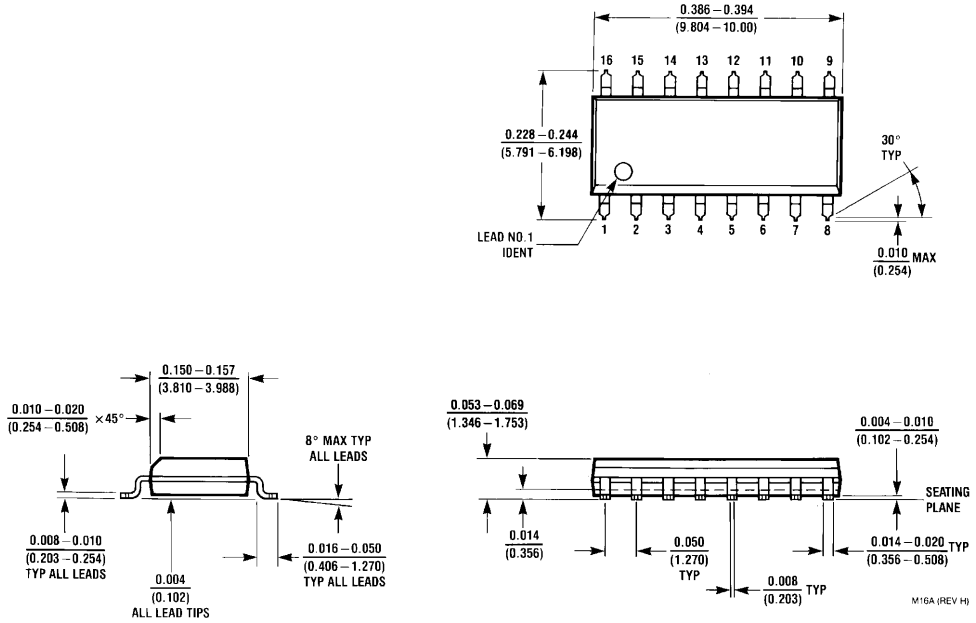
Note 7: I_{CC} is measured with 4.5V applied to all inputs and all outputs OPEN.

DM74LS158 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

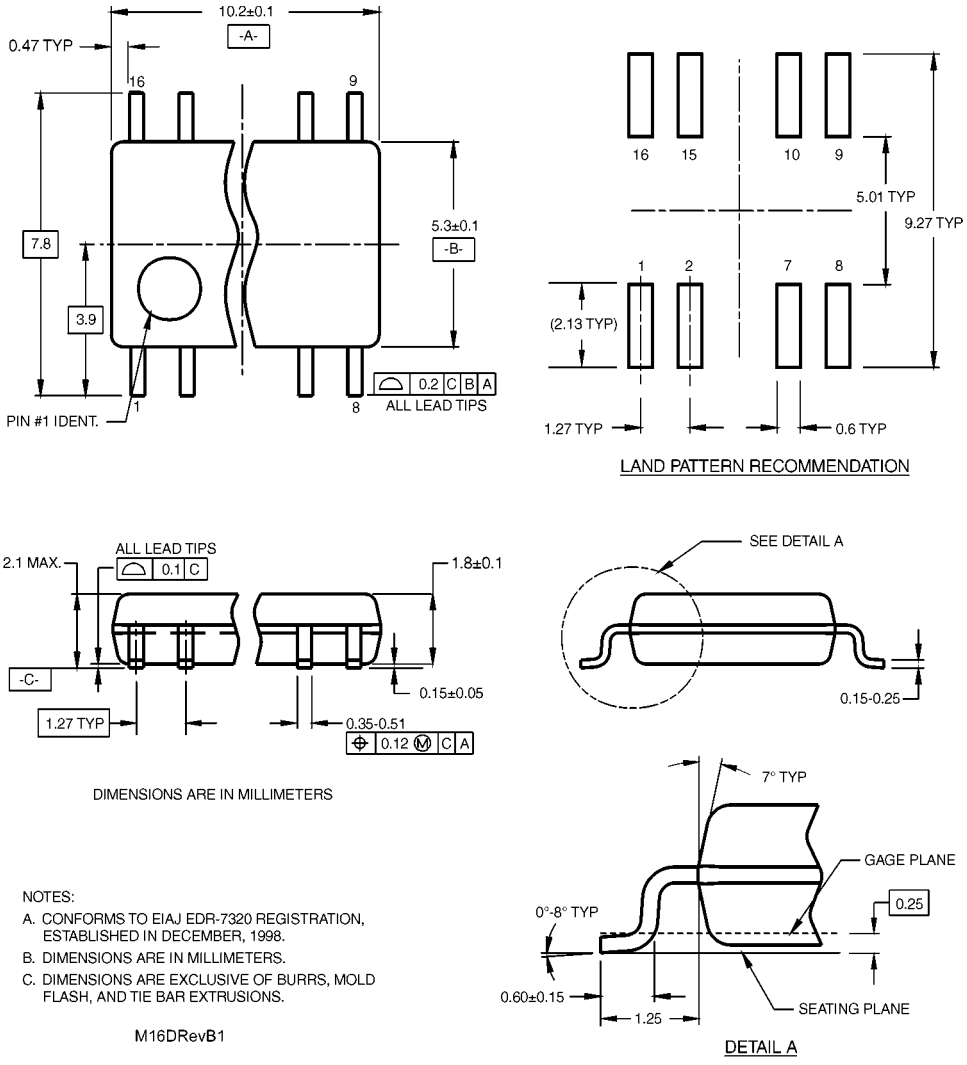
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Y		12		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Y		12		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Strobe to Y		17		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Strobe to Y		18		28	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Y		20		24	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Y		24		36	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

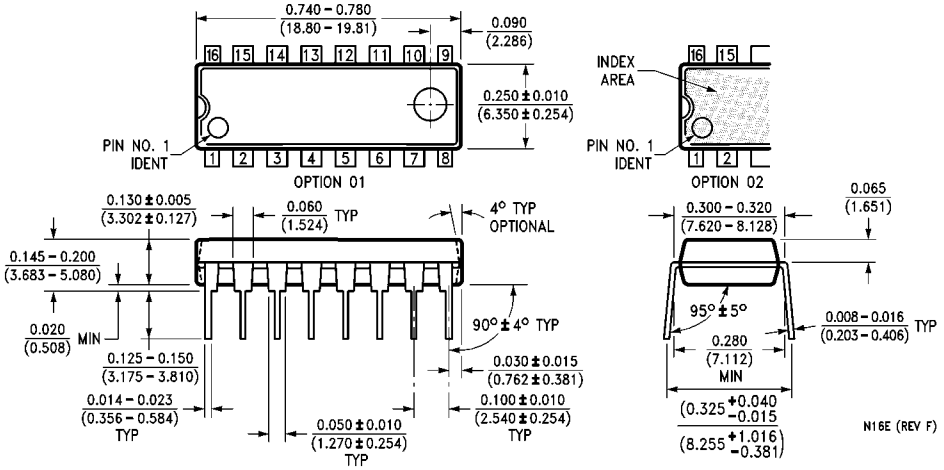
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

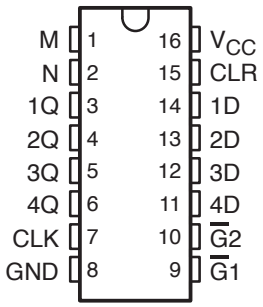


16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

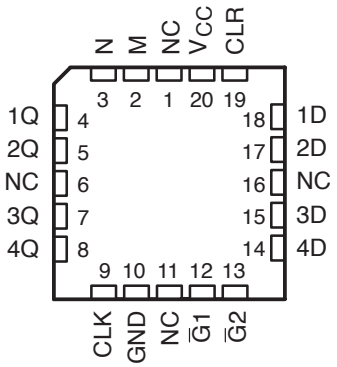
- **3-State Outputs Interface Directly With System Bus**
- **Gated Output-Control LInes for Enabling or Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:**
  - **Parallel Load**
  - **Do Nothing (Hold)**
- **For Application as Bus Buffer Registers**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY
’173	23 ns	35 MHz
’LS173A	18 ns	50 MHz

SN54173, SN54LS173A . . . J OR W PACKAGE
SN74173 . . . N PACKAGE
SN74LS173A . . . D or N PACKAGE
(TOP VIEW)



SN54LS173A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’173 and ’LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable ($\overline{G}1$, $\overline{G}2$) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

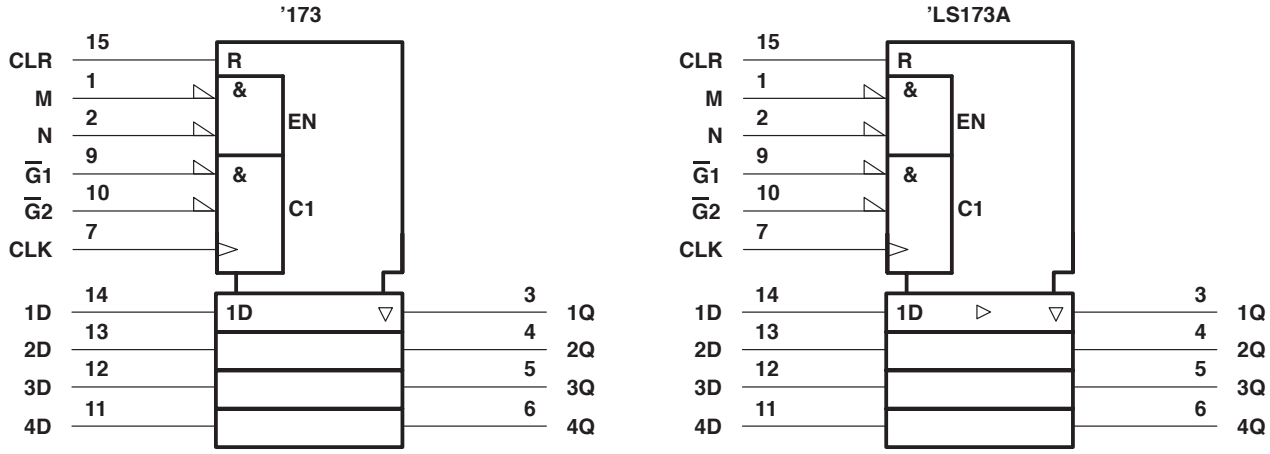
The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74173 and SN74LS173A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUT Q
CLR	CLK	DATA ENABLE $\overline{G1}$	DATA ENABLE $\overline{G2}$	DATA D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

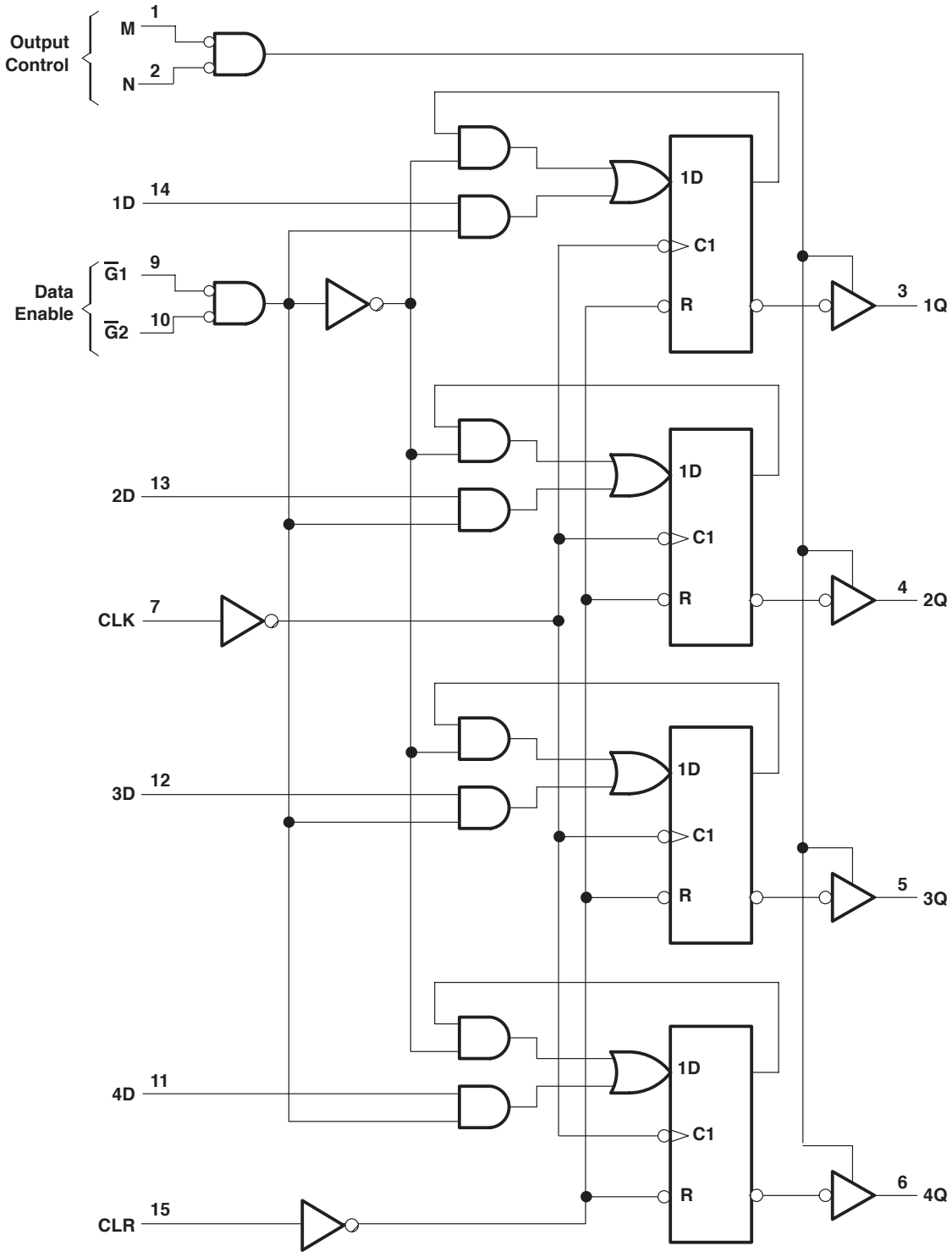
When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic symbol†



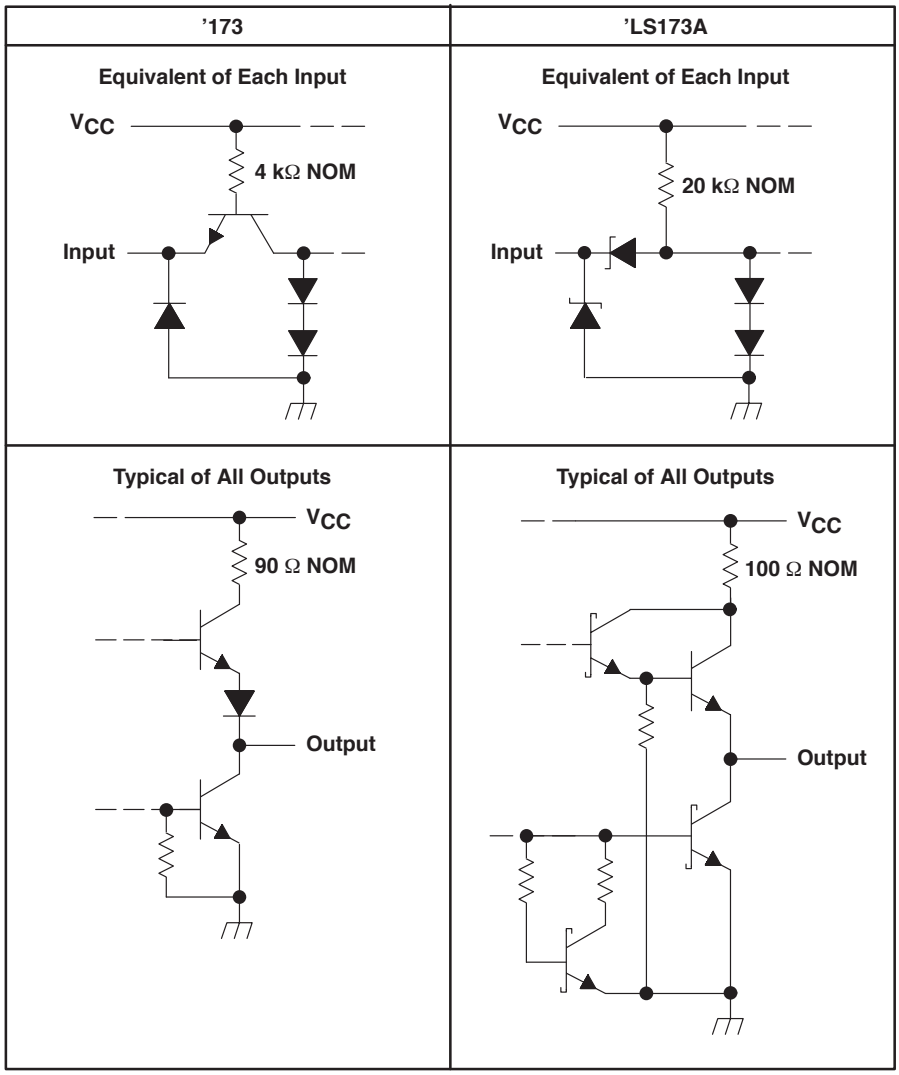
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage: '173 . . . . . –0.5 V to 5.5 V
'LS173A . . . . . –0.5 V to 7 V
Off-state output voltage . . . . . –0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			–2			–5.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54173			SN74173			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –12 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.4			0.4	V
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			150			40	μA
			V_O = 0.4 V			–150			–40	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			–1.6			–1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		–30		–70	–30		–70	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		50	72		50	72	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, $\overline{G}1$, $\overline{G}2$, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

			SN54173		SN74173		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Input clock frequency			25		25	MHz
t_w	Pulse duration	CLK or CLR	20		20		ns
t_{su}	Setup time	Data enable ($\overline{G}1$, $\overline{G}2$)	17		17		ns
		Data	10		10		
		CLR (inactive state)	10		10		
t_h	Hold time	Data enable ($\overline{G}1$, $\overline{G}2$)	2		2		ns
		Data	10		10		

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω (see Figure 1)

PARAMETER		TEST CONDITIONS	SN54173			SN74173			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum clock frequency	C_L = 50 pF	25	35		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			18	27		18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			28	43		28	43	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			19	31		19	31	
t_{PZH}	Output enable time to high level		7	16	30	7	16	30	ns
t_{PZL}	Output enable time to low level		7	21	30	7	21	30	
t_{PHZ}	Output disable time from high level	C_L = 5 pF	3	5	14	3	5	14	ns
t_{PLZ}	Output disable time from low level		3	11	20	3	11	20	

recommended operating conditions

		SN54LS173A			SN74LS173A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS173A			SN74LS173A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	V
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	V
			V_O = 0.4 V			–20			–20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			–0.4			–0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		–30		–130	–30		–130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		19	30		19	24	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, $\overline{G}1$, $\overline{G}2$, and all data inputs grounded; and CLK and M at 4.5 V.

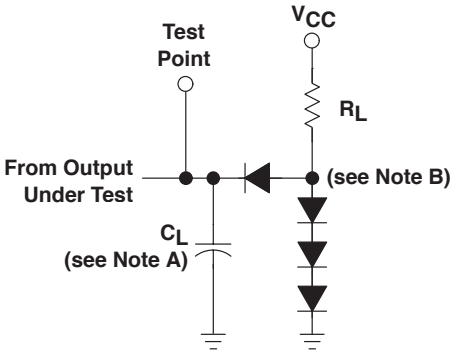
timing requirements over recommended operating conditions (unless otherwise noted)

			SN54LS173A		SN74LS173A		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Input clock frequency			30		25	MHz
t_w	Pulse duration	CLK or CLR	25		25		ns
t_{su}	Setup time	Data enable ($\overline{G}1$, $\overline{G}2$)	35		35		ns
		Data	17		17		
		CLR (inactive state)	10		10		
t_h	Hold time	Data enable ($\overline{G}1$, $\overline{G}2$)	0		0		ns
		Data	3		3		

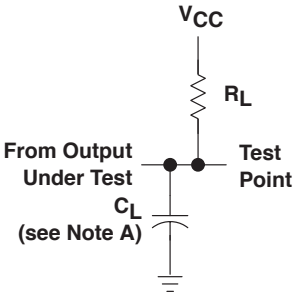
switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω (see Figure 2)

PARAMETER		TEST CONDITIONS	SN54LS173A			SN74LS173A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum clock frequency	C_L = 45 pF	30	50		30	50		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			26	35		26	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			17	25		17	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			22	30		22	30	
t_{PZH}	Output enable time to high level			15	23		15	23	ns
t_{PZL}	Output enable time to low level			18	27		18	27	
t_{PHZ}	Output disable time from high level	C_L = 5 pF		11	20		11	20	ns
t_{PLZ}	Output disable time from low level			11	17		11	17	

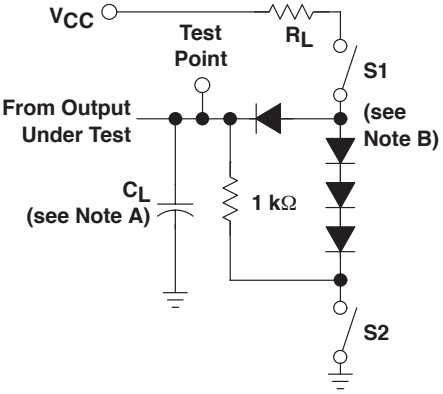
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES



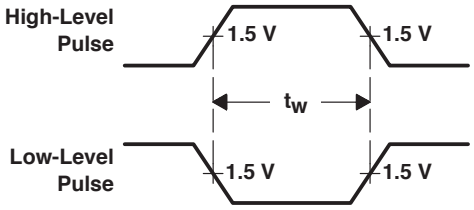
LOAD CIRCUIT
FOR 2-STATE TOTEM-POLE OUTPUTS



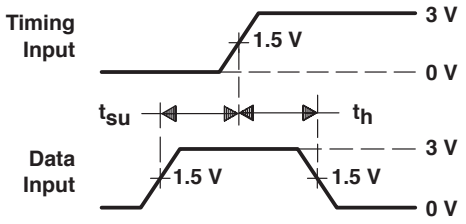
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



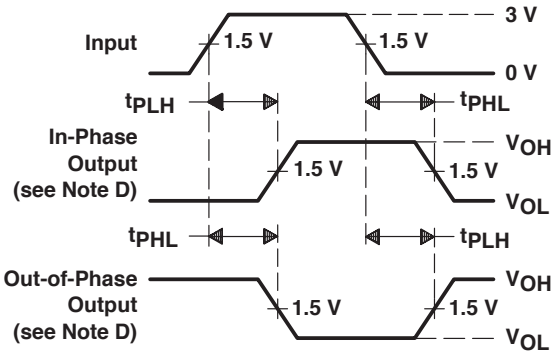
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



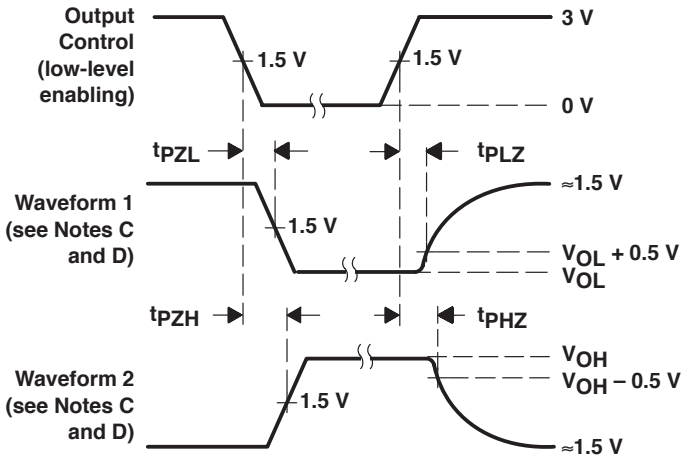
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

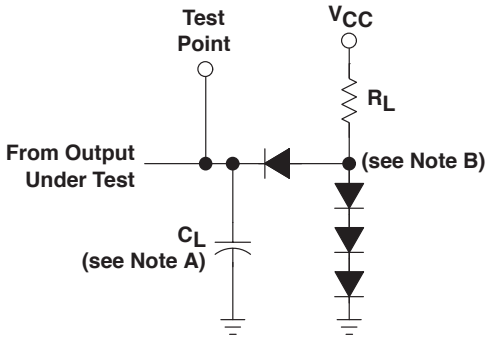


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

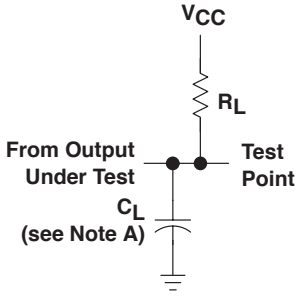
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, t_r and $t_f \le 7$ ns for Series 54/74 devices and t_r and $t_f \le 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

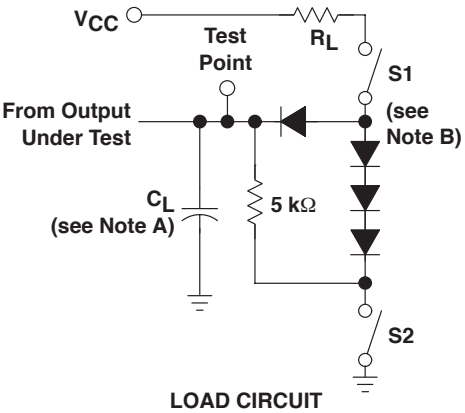
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



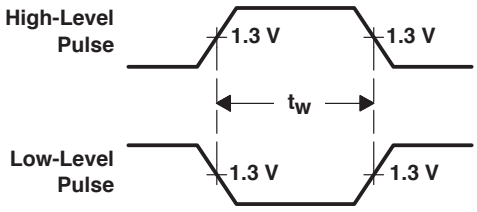
LOAD CIRCUIT FOR
2-STATE
TOTEM-POLE OUTPUTS



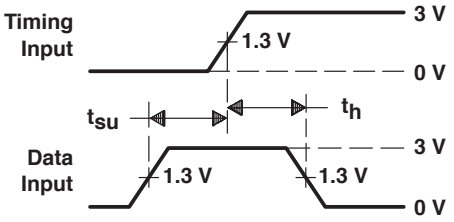
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



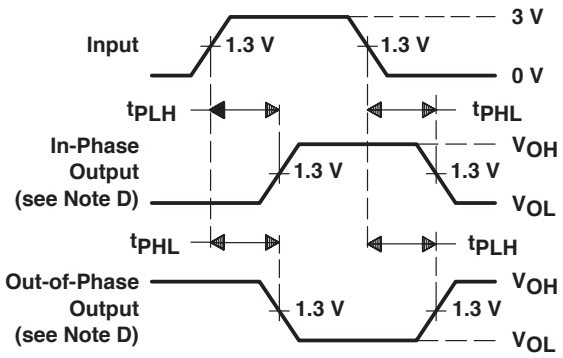
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



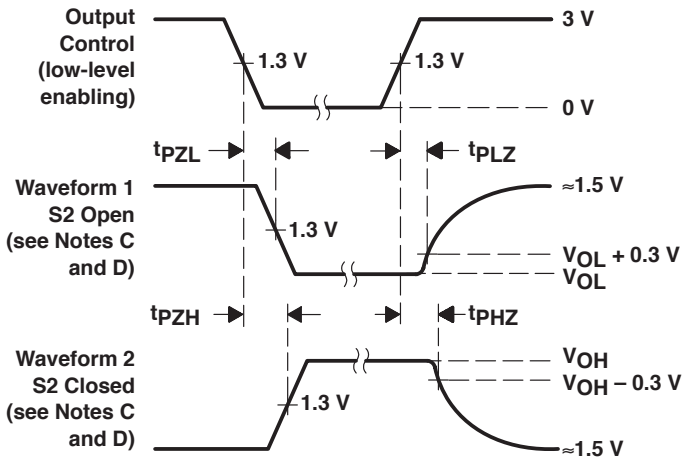
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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FAIRCHILD SEMICONDUCTOR™

April 1988
Revised June 2002

74F189
64-Bit Random Access Memory with 3-STATE Outputs

General Description

The F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-STATE and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Features

- 3-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing

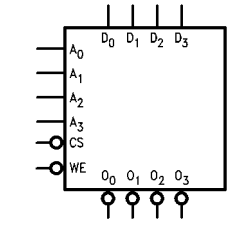
Ordering Code:

Order Number	Package Number	Package Description
74F189SC	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74F189SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F189PC (Note 1)	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

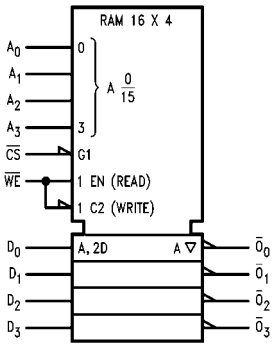
Devices also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

Note 1: This device not available in Tape and Reel.

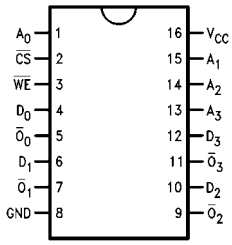
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

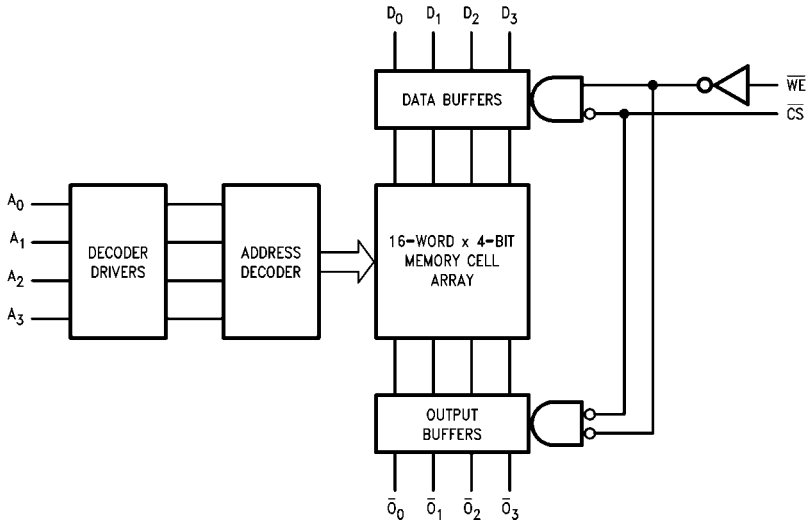
Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_3	Address Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 µA/–1.2 mA
$\overline{WE}$	Write Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
D_0–D_3	Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{O}_0$–$\overline{O}_3$	Inverted Data Outputs	150/40 (33.3)	–3.0 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		10% V_{CC}	2.4					I_{OH} = −3 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (except $\overline{CS}$)
					−1.2			V_{IN} = 0.5V ($\overline{CS}$)
I_{OZH}	Output Leakage Current				50	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V
I_{CCZ}	Power Supply Current			37	55	mA	Max	V_O = HIGH Z

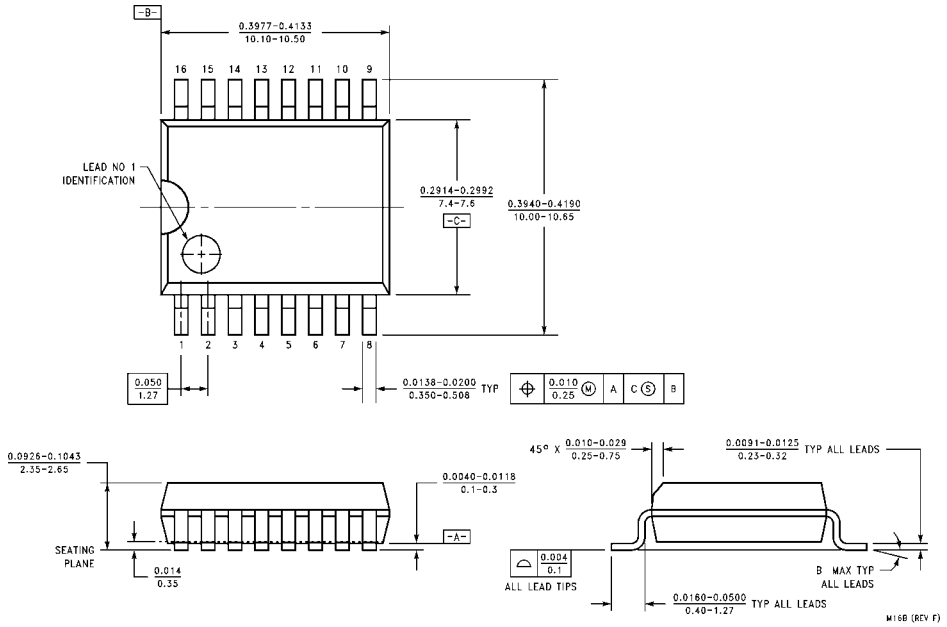
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Access Time, HIGH or LOW	10.0	18.5	26.0	9.0	32.0	10.0	27.0	ns
t_{PHL}	A_n to $\overline{O}_n$	8.0	13.5	19.0	8.0	23.0	8.0	20.0	
t_{PZH}	Access Time, HIGH or LOW	3.5	6.0	8.5	3.5	10.5	3.5	9.5	ns
t_{PZL}	$\overline{CS}$ to $\overline{O}_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0	
t_{PHZ}	Disable Time, HIGH or LOW	2.0	4.0	6.0	2.0	8.0	2.0	7.0	ns
t_{PLZ}	$\overline{CS}$ to $\overline{O}_n$	3.0	5.5	8.0	2.5	10.0	3.0	9.0	
t_{PZH}	Write Recovery Time,	6.5	15.0	28.0	6.5	37.5	6.5	29.0	ns
t_{PZL}	HIGH or LOW $\overline{WE}$ to $\overline{O}_n$	6.5	11.0	15.5	6.5	17.5	6.5	16.5	
t_{PHZ}	Disable Time, HIGH or LOW	4.0	7.0	10.0	3.5	12.0	4.0	11.0	ns
t_{PLZ}	$\overline{WE}$ to $\overline{O}_n$	5.0	9.0	13.0	5.0	15.0	5.0	14.0	

AC Operating Requirements

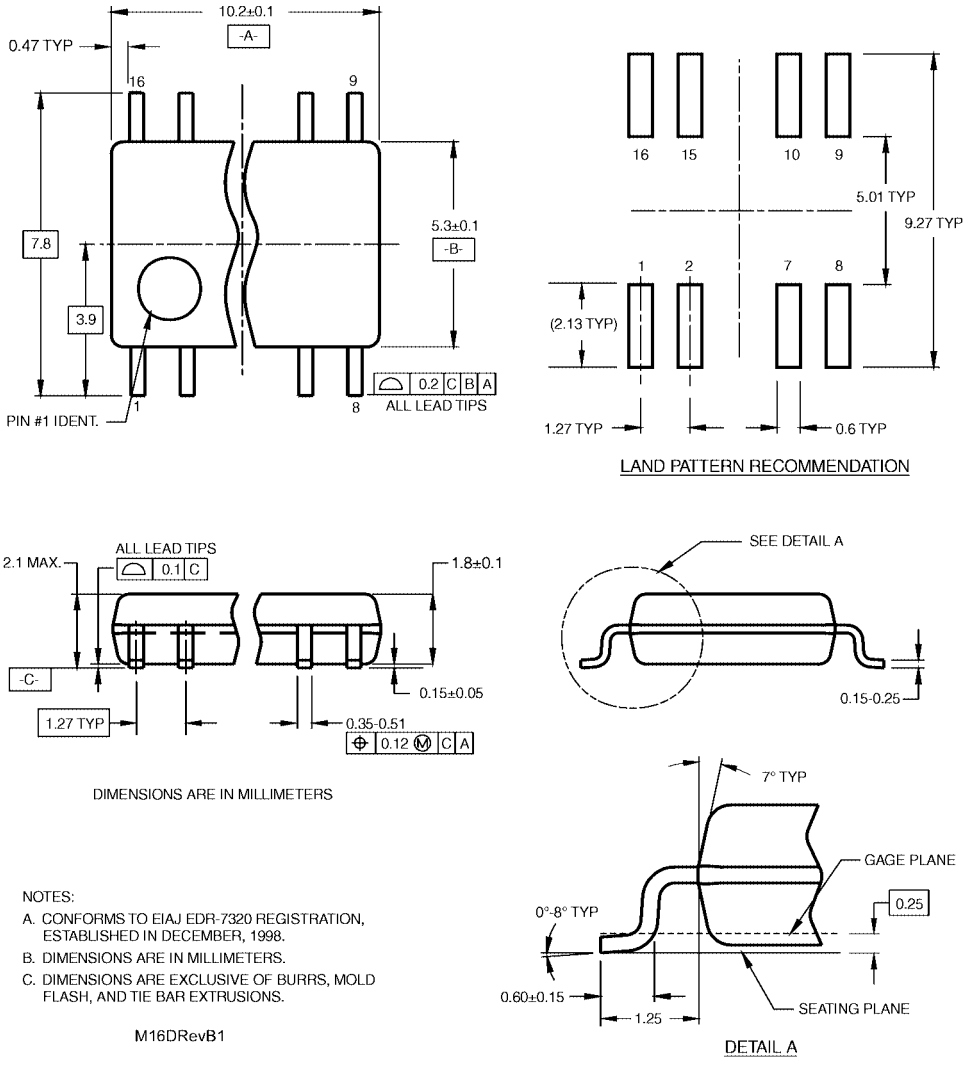
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	0		0		0		ns
$t_S(L)$	A_n to $\overline{WE}$	0		0		0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_H(L)$	A_n to $\overline{WE}$	2.0		2.0		2.0		
$t_S(H)$	Setup Time, HIGH or LOW	10.0		11.0		10.0		ns
$t_S(L)$	D_n to $\overline{WE}$	10.0		11.0		10.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		2.0		0		
$t_H(L)$	D_n to $\overline{WE}$	0		2.0		0		
$t_S(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	0		0		0		ns
$t_H(L)$	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0		7.5		6.0		
$t_W(L)$	$\overline{WE}$ Pulse Width, LOW	6.0		15.0		6.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

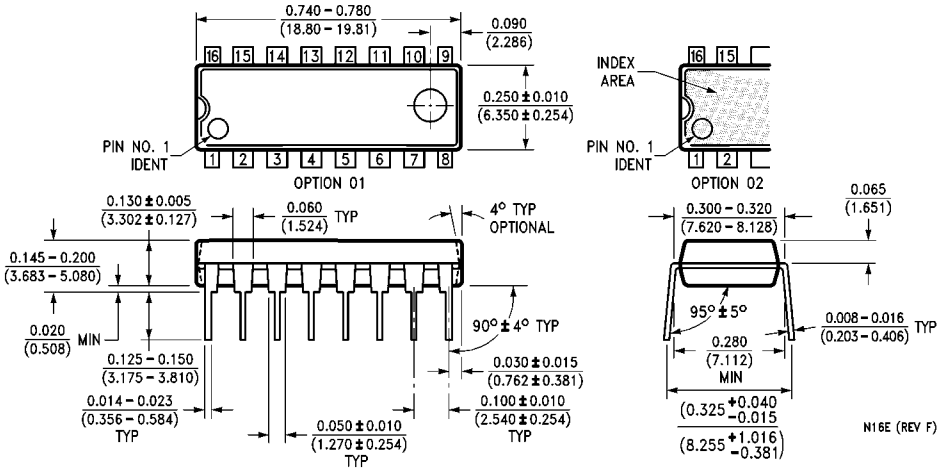
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS245
3-STATE Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A Bus to the B Bus or from the B Bus to the A Bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

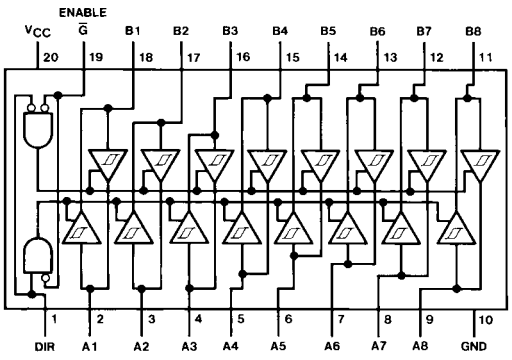
- Bi-Directional bus transceiver in a high-density 20-pin package
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  24 mA
- I_{OH} (source current)
  −15 mA

Ordering Code:

Order Number	Package Number	Package Description
DM74LS245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS245N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA			2.7			V
		V_{CC} = Min, V_{IL} = Min, V_{IL} = Max, I_{OH} = −3 mA			2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max			2			
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA				0.4	V
			I_{OL} = Max				0.5	
I_{OZH}	Off-State Output Current, HIGH Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, LOW Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or $\overline{G}$	V_I = 7V			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)			−40		−225	mA
I_{CC}	Supply Current	Outputs HIGH		V_{CC} = Max		48	70	mA
		Outputs LOW				62	90	
		Outputs at Hi-Z				64	95	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

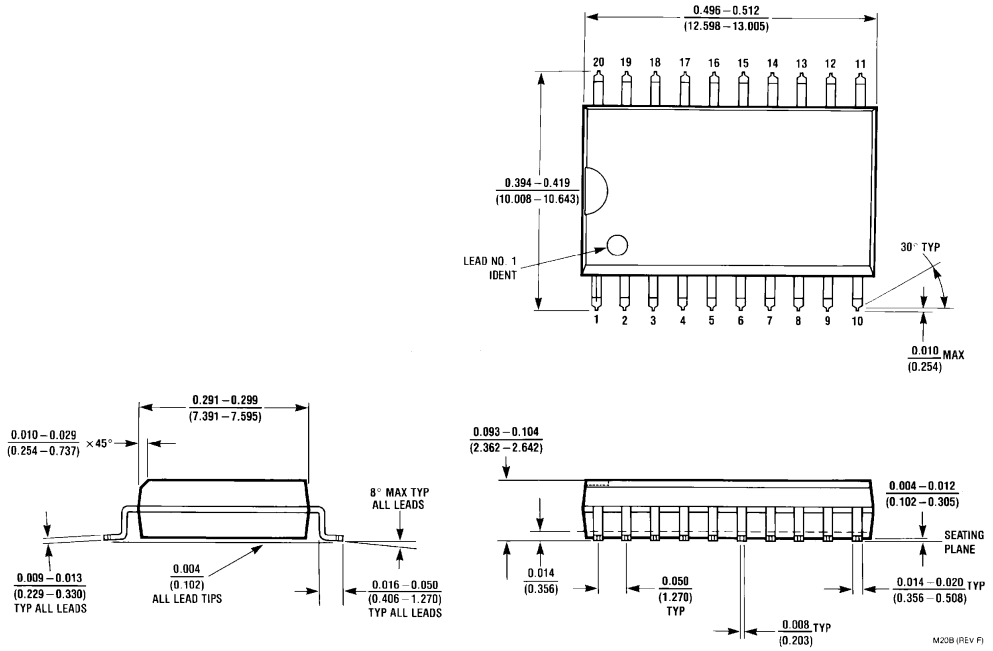
Note 3: Not more than one output should be shorted at a time, not to exceed one second duration

Switching Characteristics

V_{CC} = 5V, T_A = 25°C

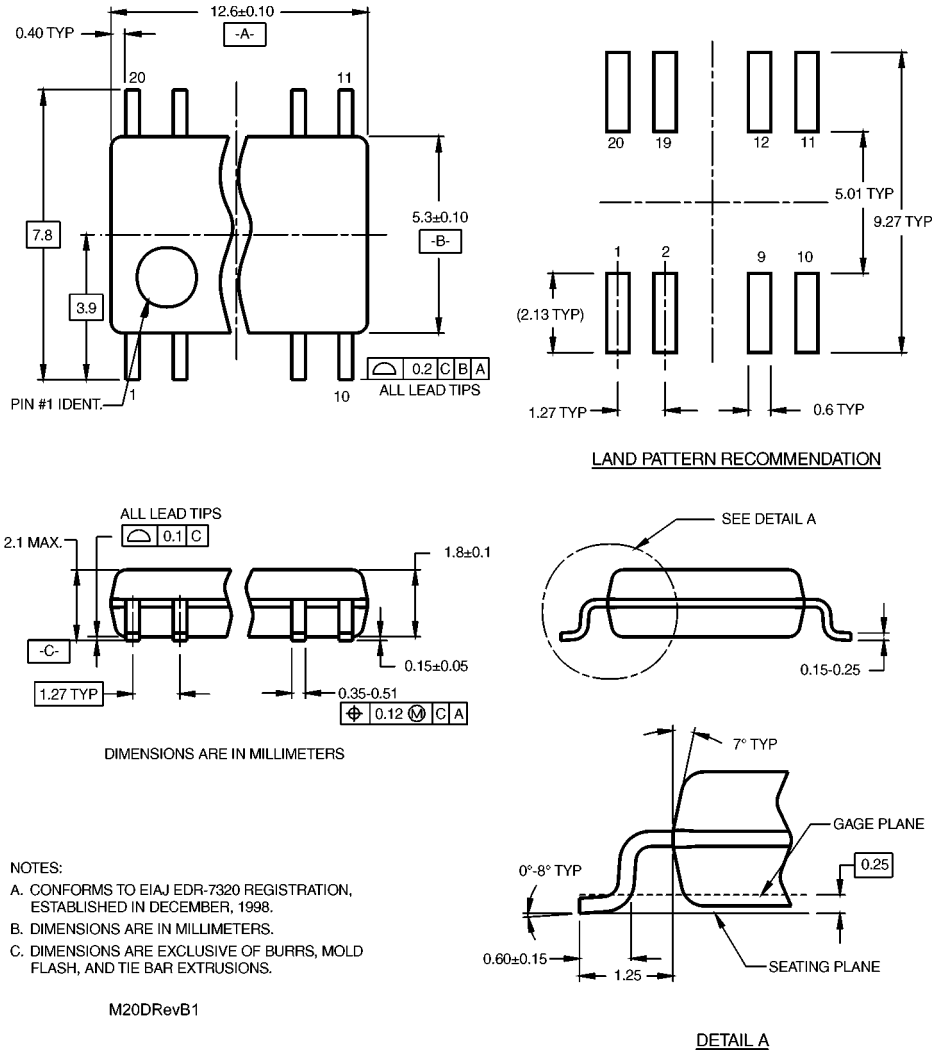
Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	C_L = 45 pF, R_L = 667Ω		12	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output			12	ns
t_{PZL}	Output Enable Time to LOW Level			40	ns
t_{PZH}	Output Enable Time to HIGH Level			40	ns
t_{PLZ}	Output Disable Time from LOW Level	C_L = 5 pF, R_L = 667Ω		25	ns
t_{PHZ}	Output Disable Time from HIGH Level			25	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	C_L = 150 pF, R_L = 667Ω		16	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output			17	ns
t_{PZL}	Output Enable Time to LOW Level			45	ns
t_{PZH}	Output Enable Time to HIGH Level			45	ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

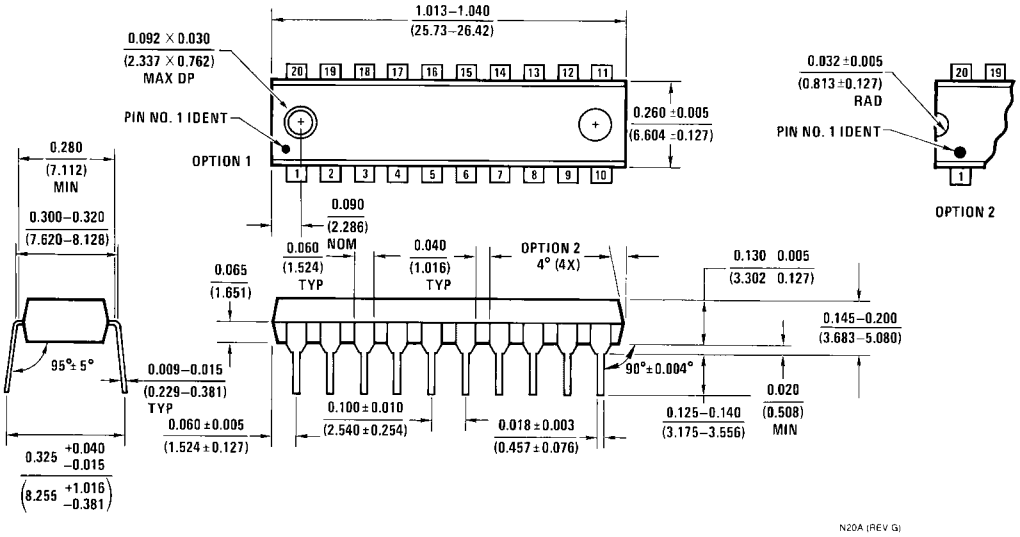
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised April 2000

DM74LS161A • DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM74LS161A and DM74LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the DM74LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs LOW, regardless of the levels of clock, load, or enable inputs. The clear function for the DM74LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs LOW after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be HIGH to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. HIGH-to-LOW level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

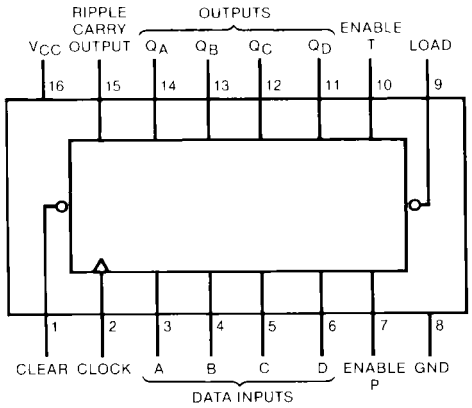
- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

Ordering Code:

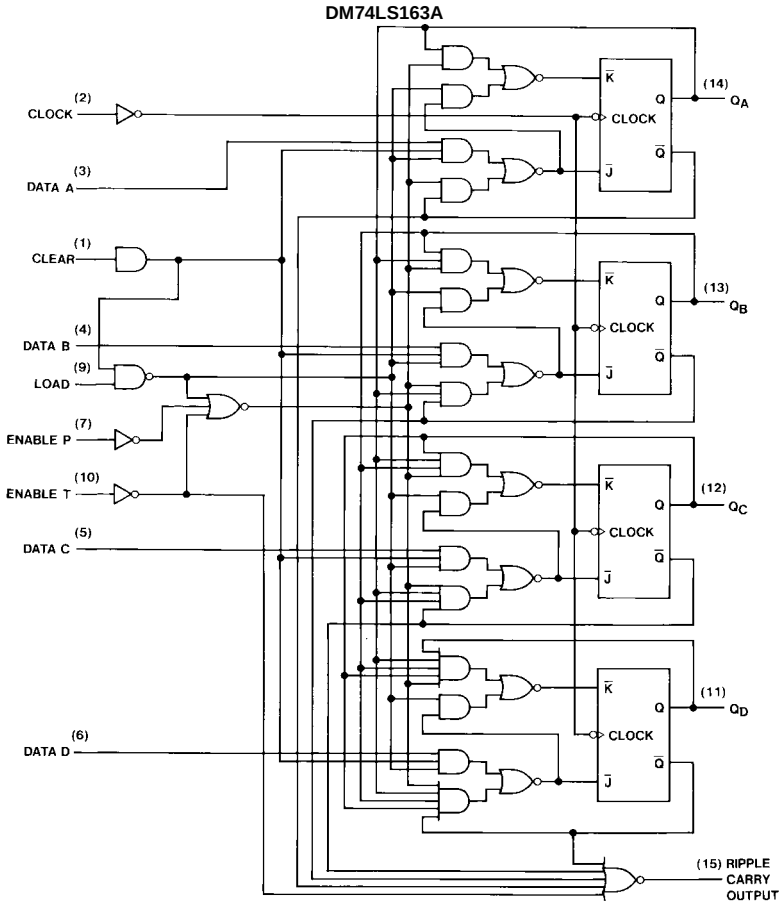
Order Number	Package Number	Package Description
DM74LS161AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS161AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS163AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS163AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



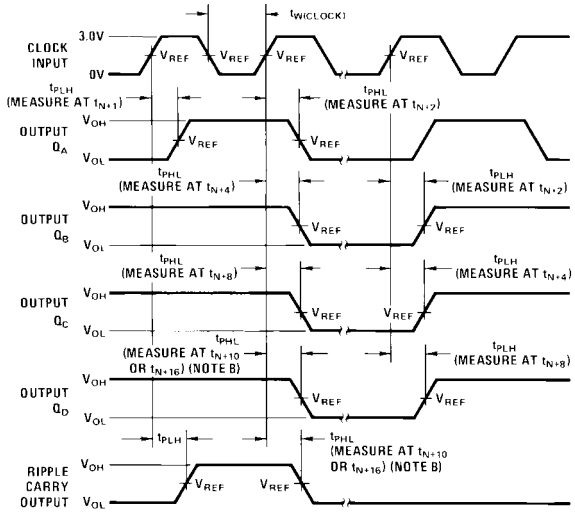
Logic Diagram



The DM74LS161A is similar, however, the clear buffer is connected directly to the flip-flops.

Parameter Measurement Information

Switching Time Waveforms



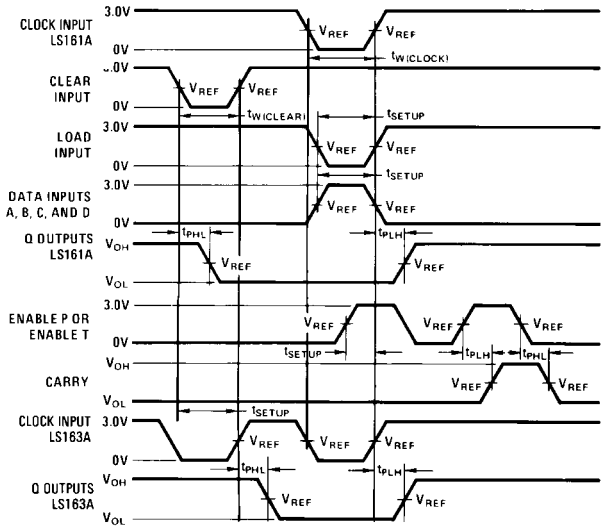
The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_R \leq 10$ ns, $t_F \leq 10$ ns.

Vary PRR to measure f_{MAX}.

Outputs Q_D and carry are tested at t_{N+16} where t_N is the bit time when all outputs are LOW.

$V_{REF} = 1.5V$.

Switching Time Waveforms



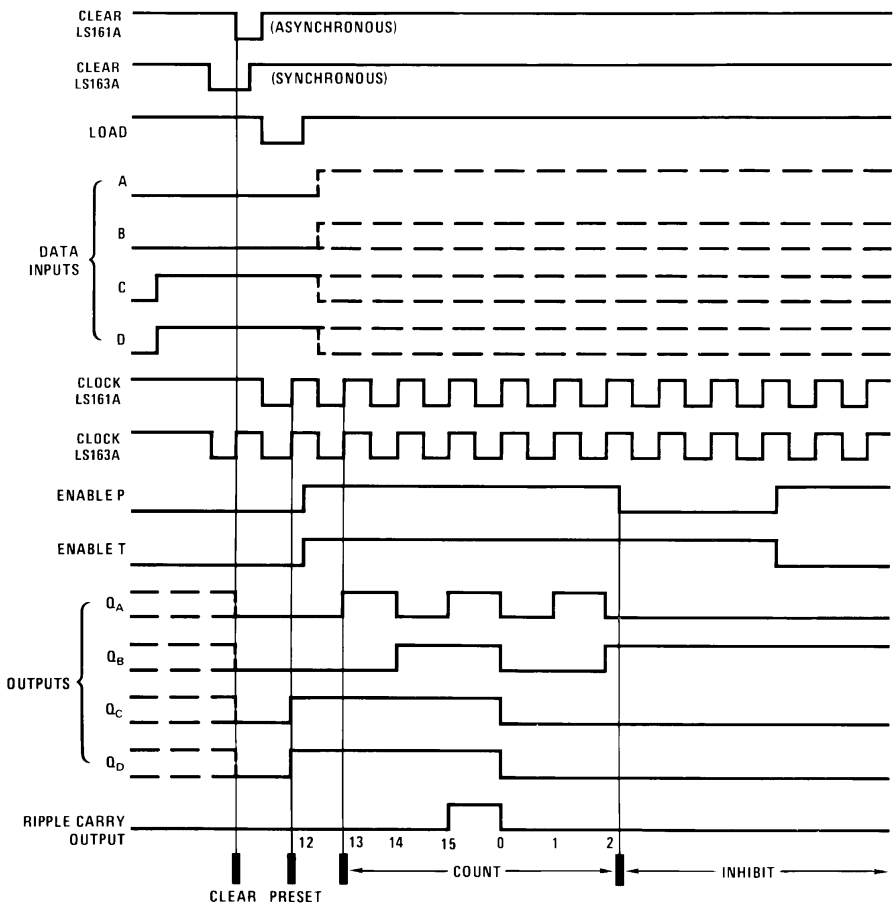
The input pulses are supplied by generators having the following characteristics:
PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_R \leq 6$ ns, $t_F \leq 6$ ns. Vary PRR to measure f_{MAX}.

Enable P and enable T setup times are measured at t_{N+0}.

$V_{REF} = 1.3V$.

Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



Sequence:

(1) Clear outputs to zero

(2) Preset to binary twelve

(3) Count to thirteen, fourteen, fifteen, zero, one, and two

(4) Inhibit

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS161A Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	MHz
	Clock Frequency (Note 3)		0		20	MHz
t_W	Pulse Width	Clock	20	6		ns
	(Note 2)	Clear	20	9		
	Pulse Width	Clock	25			ns
	(Note 3)	Clear	25			
t_{SU}	Setup Time	Data	20	8		ns
	(Note 2)	Enable P	25	17		
		Load	25	15		
	Setup Time	Data	20			ns
	(Note 3)	Enable P	30			
		Load	30			
t_H	Hold Time	Data	0	−3		ns
	(Note 2)	Others	0	−3		
	Hold Time	Data	5			ns
	(Note 3)	Others	5			
t_{REL}	Clear Release Time (Note 2)		20			ns
	Clear Release Time (Note 3)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

DM74LS161A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.7V	Enable T			40	µA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 6)			18	31	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 7)			19	32	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CCH} is measured with the load HIGH, then again with the load LOW, with all other inputs HIGH and all outputs OPEN.

Note 7: I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs OPEN.

DM74LS161A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load HIGH)		22		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load HIGH)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load LOW)		24		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load LOW)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Any Q		28		45	ns

DM74LS163A Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 8)		0		25	MHz
	Clock Frequency (Note 9)		0		20	MHz
t_W	Pulse Width	Clock	20	6		ns
	(Note 8)	Clear	20	9		
	Pulse Width	Clock	25			ns
	(Note 9)	Clear	25			
t_{SU}	Setup Time	Data	20	8		ns
	(Note 8)	Enable P	25	17		
		Load	25	15		
	Setup Time	Data	20			ns
	(Note 9)	Enable P	30			
		Load	30			
t_H	Hold Time	Data	0	−3		ns
	(Note 8)	Others	0	−3		
	Hold Time	Data	5			ns
	(Note 9)	Others	5			
t_{REL}	Clear Release Time (Note 8)		20			ns
	Clear Release Time (Note 9)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

DM74LS163A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level	V_{CC} = Min, I_{OH} = Max		2.7	3.4		V
	Output Voltage	V_{IL} = Max, V_{IH} = Min					
V_{OL}	LOW Level	V_{CC} = Min, I_{OL} = Max			0.35	0.5	V
	Output Voltage	V_{IL} = Max, V_{IH} = Min					
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max	Enable T			0.2	mA
	Input Voltage	V_I = 7V	Clock, Clear			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	HIGH Level	V_{CC} = Max	Enable T			40	µA
	Input Current	V_I = 2.7V	Load			40	
			Clock, Clear			40	
			Others			20	
I_{IL}	LOW Level	V_{CC} = Max	Enable T			−0.8	mA
	Input Current	V_I = 0.4V	Clock, Clear			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 11)		−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 12)			18	31	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 13)			18	32	mA

Note 10: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 11: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 12: I_{CCH} is measured with the load HIGH, then again with the load LOW, with all other inputs HIGH and all outputs OPEN.

Note 13: I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs OPEN.

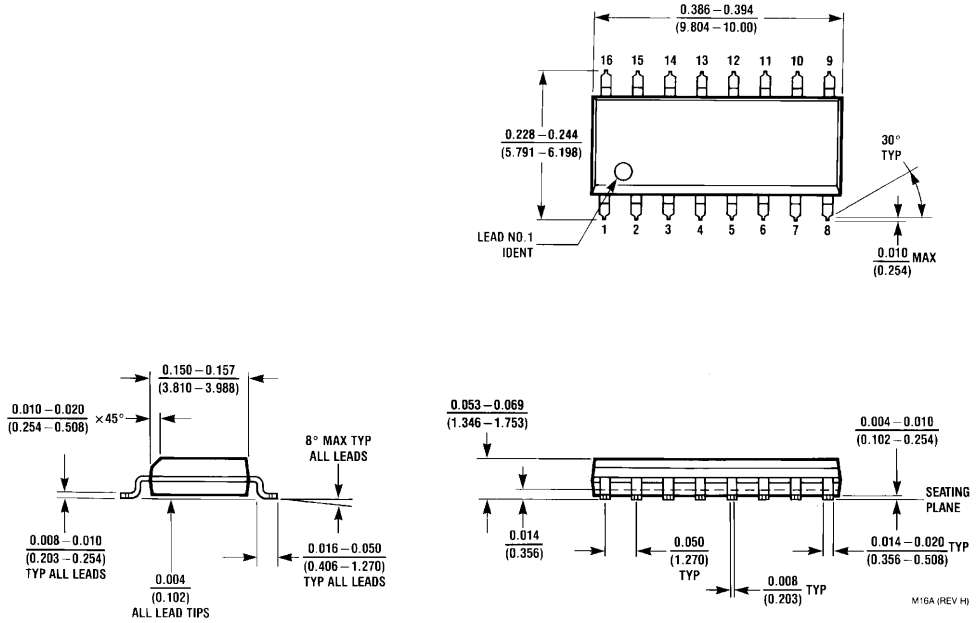
DM74LS163A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load HIGH)		22		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load HIGH)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load LOW)		24		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load LOW)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Any Q (Note 14)		28		45	ns

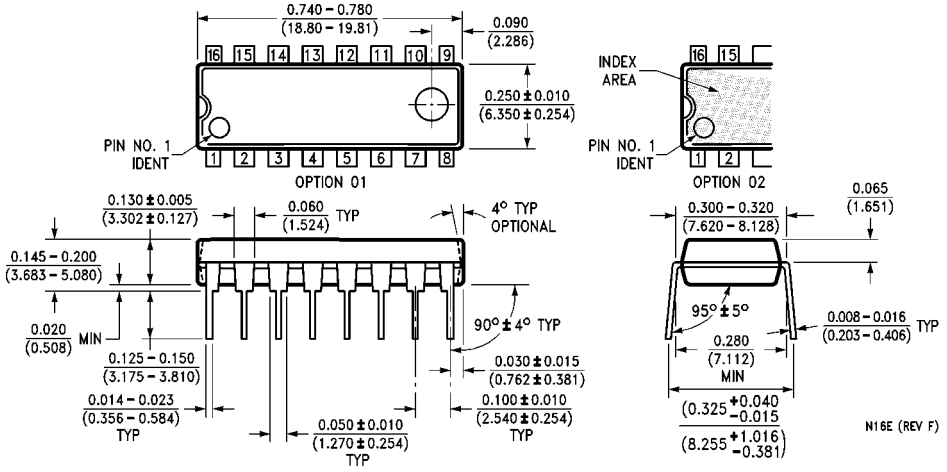
Note 14: The propagation delay clear to output is measured from the clock input transition.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E