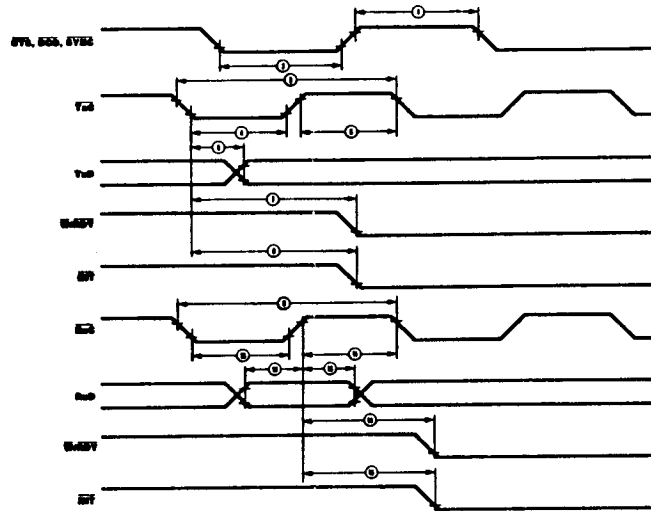


Distributed by:



www.Jameco.com ♦ 1-800-831-4242

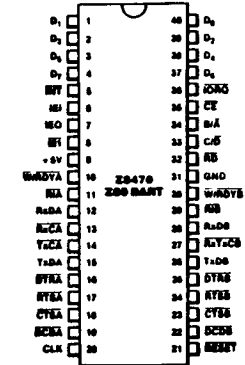
The content and copyrights of the attached material are the property of its owner.



Zilog

Z08470 Customer Procurement Spec (CPS)

GENERAL DESCRIPTION The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.



40-Pin Dual-In-Line Package (DIP), Pin Assignments

Z80 is a registered trademark of Zilog, Inc.

Copyright 1986 by Zilog, Inc.
 All rights reserved. Specifications (parameters) on products delivered in the future are subject to change without notice. All parameters are tested, except those which are characterized or guaranteed by design.

Zilog, Inc. 1315 Dell Ave., Campbell, California 95008
 Telephone (408)370-8000 TWX 910-338-7621

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Condition
V _{IL} C	Clock Input Low Voltage	-0.3 ^a	+0.45 ^a	V	
V _{IH} C	Clock Input High Voltage	V _{CC} - 0.6 ^a	+5.5 ^a	V	
V _{IL}	Input Low Voltage	-0.3 ^a	+0.8 ^a	V	
V _{IH}	Input High Voltage	+2.0 ^a	+5.5 ^a	V	
V _{OL}	Output Low Voltage		+0.4 ^a	V	I _{OL} = 2.0 mA
V _{OH}	Output High Voltage	+2.4 ^a		V	I _{OH} = -250 μA
I _{IL}	Input/3-State Output Leakage Current	-10 ^b	+10 ^b	μA	0.4 < V _{IN} < 2.4V
I _{IPB}	R _I Pin Leakage Current	-40 ^b	+10 ^b	μA	0.4 < V _{IN} < 2.4V
I _{CC}	Power Supply Current		100 ^b	mA	

V_L = 0°C to 70°C; V_{CC} = -0.5 V_{CC}

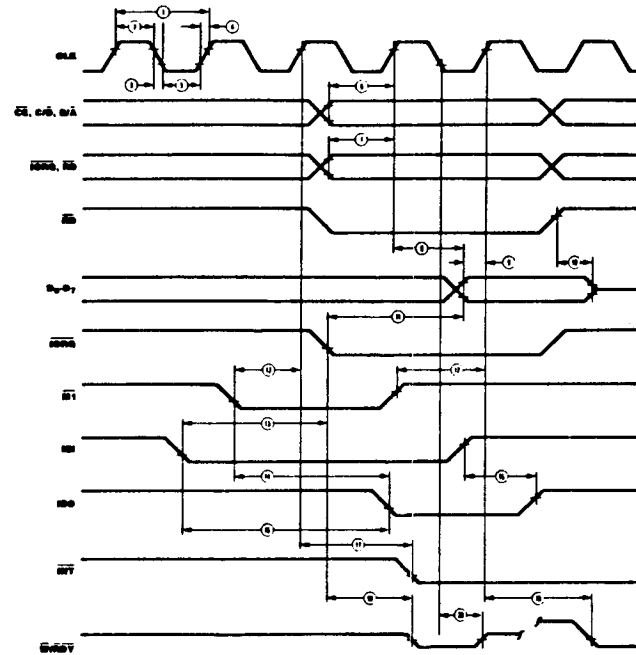
- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization

AC CHARACTERISTICS*

Number	Symbol	Parameter	Z80-4 DART		Z80-6 DART	
			Min	Max	Min	Max
1	T _{cC}	Clock Cycle Time	250 ^a	4000 ^a	165 ^a	4000 ^a
2	T _{cH}	Clock Width (High)	105 ^a	2000 ^a	70 ^a	2000 ^a
3	T _{cF}	Clock Fall Time		30 ^a		15 ^a
4	T _{cR}	Clock Rise Time		30 ^a		15 ^a
5	T _{cL}	Clock Width (Low)	105 ^a	2000 ^a	70 ^a	2000 ^a
6	T _{sAD(C)}	CE, C/Σ, B/A to Clock ↑ Setup Time	145 ^b		80 ^b	
7	T _{sCS(C)}	IORC, RD to Clock ↑ Setup Time	115 ^b		80 ^b	
8	T _{dC(DO)}	Clock ↑ to Data Out Delay		220 ^b		150 ^b
9	T _{dC(C)}	Data In to Clock ↑ Setup (Write or M1 Cycle)	50 ^b		30 ^b	
10	T _{dRD(DOz)}	RD ↑ to Data Out Float Delay		110 ^c		90 ^c
11	T _{dO(DOz)}	IORC ↓ to Data Out Delay (NTACK Cycle)		180 ^c		100 ^c
12	T _{sM1(C)}	M1 to Clock ↑ Setup Time	90 ^b		75 ^b	
13	T _{sIE(EO)}	IE1 to IORC ↓ Setup Time (NTACK Cycle)	140 ^c		120 ^c	
14	T _{dM1(EO)}	M1 ↓ to EO ↓ Delay (interrupt before M1)		180 ^c		180 ^c
15	T _{dIE(EOz)}	IE1 ↑ to EO ↓ Delay (after ED decode)		100 ^c		70 ^c
16	T _{dIE(EOz)}	IE1 ↓ to EO ↓ Delay		100 ^b		70 ^b
17	T _{dC(NT)}	Clock ↑ to INT ↓ Delay		200 ^b		150 ^b
18	T _{dC(WRRW)}	IORC ↓ or CE ↓ to W/RDY ↓ Delay (Wait Mode)		210 ^c		175 ^c
19	T _{dC(WRR)}	Clock ↑ to W/RDY ↓ Delay (Ready Mode)		120 ^b		100 ^c
20	T _{dC(WRRz)}	Clock ↓ to W/RDY Float Delay (Wait Mode)		130 ^c		110 ^c

*Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization



AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	Z80-4 DART		Z80-6 DART		Notes*
			Min	Max	Min	Max	
1	T _{wPh}	Pulse Width (High)	200 ^c		200 ^c		2
2	T _{wPl}	Pulse Width (Low)	200 ^c		200 ^c		2
3	T _{cTc}	ΣC Cycle Time	400 ^c	∞ ^c	330 ^c	∞ ^c	2
4	T _{wTcL}	ΣC Width (Low)	180 ^c	∞ ^c	100 ^c	∞ ^c	2
5	T _{wTcH}	ΣC Width (High)	180 ^c	∞ ^c	100 ^c	∞ ^c	2
6	T _{dTc(TxD)}	ΣC ↓ to TxD Delay		300 ^b		220 ^b	2
7	T _{dTc(WRR)}	ΣC ↓ to W/RDY ↓ Delay (Ready Mode)	5 ^c	9 ^c	5 ^c	9 ^c	1
8	T _{dTc(INT)}	ΣC ↓ to INT ↓ Delay	5 ^c	9 ^c	5 ^c	9 ^c	1
9	T _{cRxC}	RxC Cycle Time	400 ^c	∞ ^c	330 ^c	∞ ^c	2
10	T _{wRxC}	RxC Width (Low)	180 ^c	∞ ^c	100 ^c	∞ ^c	2
11	T _{wRxC}	RxC Width (High)	180 ^c	∞ ^c	100 ^c	∞ ^c	2
12	T _{sRxD(RxC)}	RxD to RxC ↑ Setup Time (x1 Mode)	0 ^c		0 ^c		2
13	T _{hRxD(RxC)}	RxD Hold Time (x1 Mode)	140 ^c		100 ^c		2
14	T _{dRxC(WRR)}	RxC ↑ to W/RDY ↓ Delay (Ready Mode)	10 ^c	13 ^c	10 ^c	13 ^c	1
15	T _{dRxC(NT)}	RxC ↑ to INT ↓ Delay	10 ^c	13 ^c	10 ^c	13 ^c	1

* In all modes, the System Clock rate must be at least five times the maximum data rate. RESET must be active a minimum of one complete clock cycle.

1 Units equal to System Clock Periods.

2 Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization