

16-BIT MICROPROCESSOR

TMP68HC000P-10 / TMP68HC000P-12 / TMP68HC000P-16
 TMP68HC000N-10 / TMP68HC000N-12 / TMP68HC000N-16
 TMP68HC000Y-10 / TMP68HC000Y-12 / TMP68HC000Y-16
 TMP68HC000F-10 / TMP68HC000F-12 / TMP68HC000F-16
 TMP68HC000T-10* / TMP68HC000T-12* / TMP68HC000T*-16

Package type :

P : plastic DIP
 N : Shrank plastic DIP
 Y : pin grid array (without stand-off) : TMP68HC000 only
 F : plastic QFP : TMP68HC000 only
 T : plastic leaded chi carrier

(* Under development)

1. INTRODUCTION

TMP68HC000 are compatible with the Motorola MC68HC000.

- Low power Dissipation (TMP68HC000)

As show in the user programming model (Figure 1.1) , the TMP68HC000 offers 16/32-bit registers and a 32-bit program counter. The first eight registers (D0~D7) are used as data registers for byte (8-bit) , word (16-bit) , and long word (32-bit) operations. The second set of seven registers (A0~A6) and the user stack pointer (USP) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 16 registers may be used as index registers.

In supervisor mode, the upper byte of the status register and the supervisor stack pointer (SSP) are also available to the programmer. These registers are shown in Figure 1.2.

The status register (Figure 1.3) contains the interrupt mask (eight levels available) as well as the condition codes: extend (X) , negative (N) , zero (Z) , overflow (V) , and carry (C) . Additional status bits indicate that the processor is in a trace (T) mode and in a supervisor (S) or user state.

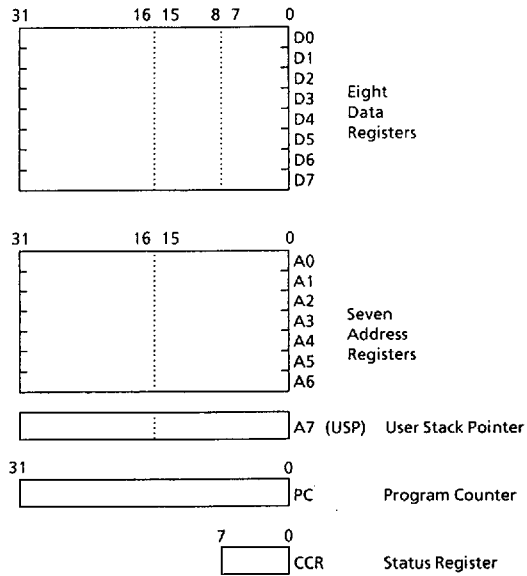


Figure 1.1 User Programming Model

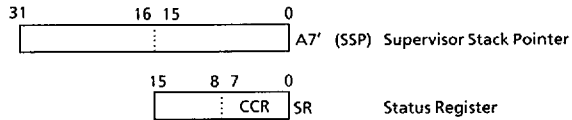


Figure 1.2 Supervisor Programming Model Supplement

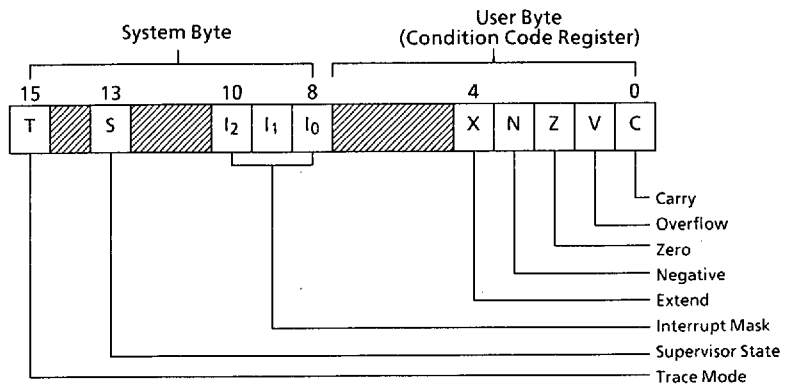


Figure 1.3 Status Register

1.1 DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4 bits)
- Bytes (8 bits)
- Words (16 bits)
- Long Words (32 bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided in the instruction set.

The 14 address modes, shown in Table 1.1, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Program Counter Relative
- Immediate
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

Table 1.1 Addressing Modes

Addressing Modes	Syntax
<u>Register Direct Addressing</u> Data Register Direct Address Register Direct	Dn An
<u>Absolute Data Addressing</u> Absolute Short Absolute Long	Abs.W Abs.L
<u>Program Counter Relative Addressing</u> Relative with Offset Relative with Index Offset	d16 (PC) d8 (PC, Xn)
<u>Register Indirect Addressing</u> Register Indirect Postincrement Register Indirect Predecrement Register Indirect Register Indirect with Offset Indexed Register Indirect with Offset	(An) (An) + -(An) d16 (An) d8 (An, Xn)
<u>Immediate Data Addressing</u> Immediate Quick Immediate	#xxx #1~#8
<u>Implied Addressing</u> Implied Register	SR / USP / SSP / PC

- Notes: Dn = Data Register
 An = Address Register
 Xn = Address or Data Register used as Index Register
 SR = Status Register
 PC = Program Counter
 SP = Stack Pointer
 USP = User Stack Pointer
 () = Effective Address
 d8 = 8-Bit Offset (Displacement)
 d16 = 16-Bit Offset (Displacement)
 #xxx = Immediate Data

1.2 INSTRUCTION SET OVERVIEW

The TMP68HC000 instruction set is shown in Table 1.2. Some additional instructions are variations, or subsets, of these and they appear in Table 1.3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned, multiply and divide, "quick" arithmetic operations, BCD arithmetic, and expanded operations (through traps).

Table 1.2 Instruction Set Summary (1/2)

Mnemonic	Description
ABCD ADD AND ASL ASR	Add Decimal with Extend Add Logical And Arithmetic Shift Left Arithmetic Shift Right
Bcc BCHG BCLR BRA BSET BSR BTST	Branch Conditionally Bit Test and Change Bit Test and Clear Branch Always Bit Test and Set Branch to Subroutine Bit Test
CHK CLR CMP	Check Register Against Bounds Clear Operand Compare
DBcc DIVS DIVU	Test Condition, Decrement and Branch Signed Divide Unsigned Divide
EOR EXG EXT	Exclusive Or Exchange Registers Sign Extend
JMP JSR	Jump Jump to Subroutine
LEA LINK LSL LSR	Load Effective Address Link Stack Logical Shift Left Logical Shift Right

Table 1.2 Instruction Set Summary (2/2)

Mnemonic	Description
MOVE MOVEM MOVEP MULS MULU	Move Move Multiple Registers Move Peripheral Data Signed Multiply Unsigned Multiply
NBCD NEG NOP NOT	Negate Decimal with Extend Negate No Operation One's Complement
OR	Logical OR
PEA	Push Effective Address
RESET ROL ROR ROXL ROXR RTE RTR RTS	Reset External Devices Rotate Left without Extend Rotate Right without Extend Rotate Left with Extend Rotate Right with Extend Return from Exception Return and Restore Return from Subroutine
STOP SUB SWAP	Stop Subtract Swap Data Register Halves
TAS TRAP TRAPV TST	Test and Set Operand Trap Trap on Overflow Test
UNLK	Unlink

Table 1.3 Variations of Instruction Types

Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR ANDI to SR	Logical And AND Immediate AND Immediate to Condition Codes AND Immediate to Status Register
CMP	CMP CMPA CMPM CMPI	Compare Compare Address Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive OR Exclusive OR Immediate Exclusive OR Immediate to Condition Codes Exclusive OR Immediate to Status Register
MOVE	MOVE MOVEA MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Move Address Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR ORI to SR	Logical OR OR Immediate OR Immediate to Condition Codes OR Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract with Extend

8. ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the TMP68000 and TMP68HC000.

8.1 MAXIMUM RATINGS

Rating	Symble	Value		Unit
		TMP68000	TMP68HC000	
Supply Voltage	V _{cc}	-0.3~ +7.0	-0.3~ +6.5	V
Input Voltage	V _{in}	-0.3~ +7.0	-0.3~ +6.5	V
Operating Temperature Range	T _a	0~ +70	0~ +70	°C
Storage Temperature	T _{stg}	-55~ +150	-55~ +150	°C

This device contains circitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{cc}).

8.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, T_a = 0°C ~ +70°C ; see Figures 8.1)

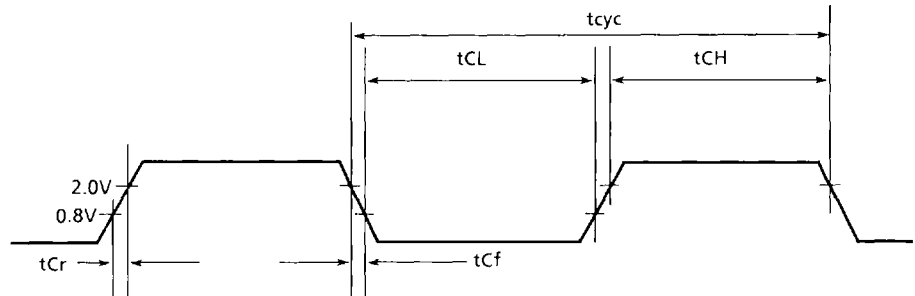
Characteristic	Symbol	TMP68000		TMP68HC000		Unit
		Min	Max	Min	Max	
Input High Voltage	V _{IH}	2.0	V _{CC}	2.0	V _{CC}	V
Input Low Voltage	V _{IL}	GND-0.3	0.8	GND-0.3	0.8	V
Input Leakage Current (5.25V)	I _{IN}	-	2.5	-	2.5	μA
		-	2.5	-	2.5	
		-	20	-	20	
Three-State (Off State) Input Current	I _{TSI}	-	20	-	20	μA
		-	20	-	20	
		-	20	-	20	
Output High Voltage (I _{OH} = -400μA)	V _{OH}	V _{CC} -0.75	-	-	-	V
		2.4	-	V _{CC} -0.75	-	
		2.4	-	V _{CC} -0.75	-	
		2.4	-	V _{CC} -0.75	-	
		2.4	-	V _{CC} -0.75	-	
Output Low Voltage (I _{OL} = 1.6mA)	V _{OL}	-	0.5	-	0.5	V
(I _{OL} = 3.2mA)		-	0.5	-	0.5	
(I _{OL} = 5.0mA)		-	0.5	-	0.5	
(I _{OL} = 5.3mA)		-	0.5	-	0.5	
		-	0.5	-	0.5	
Current Dissipation***	I _D	-	-	-	25	mA
		-	-	-	30	
		-	-	-	35	
		-	-	-	50	
Power Dissipation	P _D	-	1.5	-	0.13	W
		-	1.5	-	0.16	
		-	1.5	-	0.19	
		-	-	-	0.26	
Capacitance (V _{in} = 0V, T _a = 25°C : Frequency = 1MHz)**	C _{IN}	-	20.0	-	20.0	pF
Load Capacitance	C _L	-	70	-	70	pF
		-	130	-	130	

* : With external pullup resistor of 1.1kΩ.

** : Capacitance is periodically sampled rather than 100% tested.

*** : During normal operation instantaneous V_{CC} current requirements may be as high as 1.5 A.

8.3 AC ELECTRICAL SPECIFICATIONS – CLOCK TIMING



Note: Timing measurements are referenced to and from a low voltage of 0.8 volt and high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

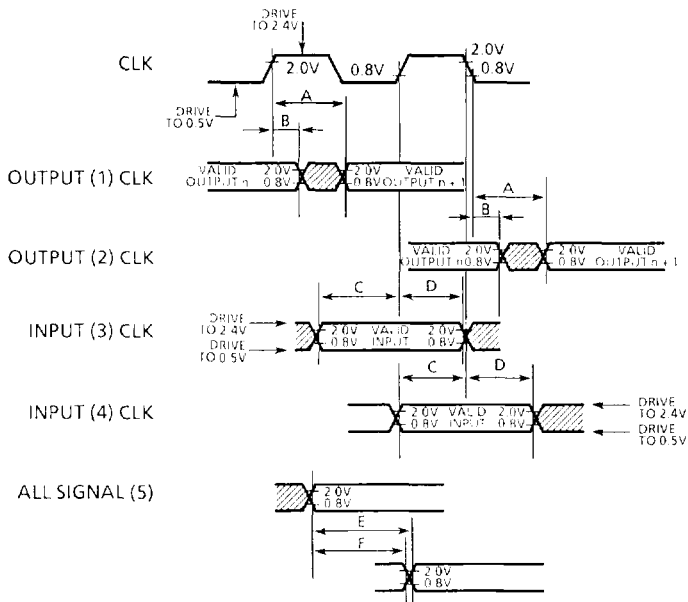
Figure 8.1 Clock Input Timing Diagram

8.4 AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 8.2. In order to test the parameters guaranteed by TOSHIBA, inputs must be driven to the voltage levels specified in this figure. Outputs are specified with minimum and / or maximum limits, as appropriate, and are measured as shown in Figure 8.2. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications are also shown.

Note: The testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



Notes :

- 1 This output timing is applicable to all parameters specified relative to the rising edge of the clock.
- 2 This output timing is applicable to all parameters specified relative to the falling edge of the clock.
- 3 This input timing is applicable to all parameters specified relative to the rising edge of the clock.
- 4 This input timing is applicable to all parameters specified relative to the falling edge of the clock.
- 5 This timing is applicable to all parameters specified relative to the assertion / negation of another signal.

Legend :

- A Maximum output delay specification.
- B Minimum output hold time.
- C Minimum input setup time specification.
- D Minimum input hold time specification.
- E Signal valid to signal valid specification (maximum or minimum) .
- F Signal valid to signal invalid specification (maximum to minimum) .

Figure 8.2 Drive Levels and Test Points for AC Specifications

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (1/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	tCYC	125	250	100	250	80	250	60	125	ns
2	Clock Width Low	tCL	55	125	45	125	35	125	27	62.5	ns
3	Clock Width High	tCH	55	125	45	125	35	125	27	62.5	ns
4	Clock Fall Time	tCf	-	10	-	10	-	5	-	5	ns
5	Clock Rise Time	tCr	-	10	-	10	-	5	-	5	ns
6	Clock Low to Address Valid	tCLAV	-	62	-	50	-	50	-	30	ns
6A	Clock High to FC Valid	tCHFCV	-	62	-	50	-	45	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	tCHADZ	-	80	-	70	-	60	-	50	ns
8	Clock High to Address, FC Invalid (Minimum)	tCHAFI	0	-	0	-	0	-	0	-	ns
91	Clock High to \overline{AS} , \overline{DS} Low	tCHSL	3	60	3	50	3	40	3	30	ns
112	Address Valid to \overline{AS} , \overline{DS} Low (Read) / \overline{AS} Low (Write)	tAVSL	30	-	20	-	15	-	15	-	ns
11A2	FC Valid to \overline{AS} , \overline{DS} Low (Read) / \overline{AS} Low (Write)	tFCVSL	90	-	70	-	60	-	45	-	ns
121	Clock Low to \overline{AS} , \overline{DS} High	tCLSH	-	62	-	50	-	40	3	30	ns
132	\overline{AS} , \overline{DS} High to Address / FC Invalid	tSHAFI	40	-	30	-	20	-	15	-	ns
142	\overline{AS} , \overline{DS} Width Low (Read) / \overline{AS} Low (Write)	tSL	270	-	195	-	160	-	120	-	ns
14A	\overline{DS} Width Low (Write)	tDSL	140	-	95	-	80	-	60	-	ns
152	\overline{AS} , \overline{DS} Width High	tSH	150	-	105	-	65	-	60	-	ns

* : 68HC000 only

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (2/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
16	Clock High to Control Bus High Impedance	tCHCZ	-	80	-	70	-	60	-	50	ns
17 ²	\overline{AS} , \overline{DS} , High to R/ \overline{W} High (Read)	tSHRH	40	-	30	-	20	-	15	-	ns
18 ¹	Clock High to R / \overline{W} High	tCHRH	0	55	0	45	0	40	0	30	ns
20 ¹	Clock High to R / \overline{W} Low (Write)	tCHRL	0	55	0	45	0	40	0	30	ns
20A2.6	\overline{AS} Low to R/ \overline{W} Valid (Write)	tASRV	-	10	-	10	-	10	-	10	ns
21 ²	Address Valid to R / \overline{W} Low (Write)	tAVRL	20	-	0	-	0	-	0	-	ns
21A ²	FC Valid to R / \overline{W} Low (Write)	tFCVRL	60	-	50	-	30	-	30	-	ns
22 ²	R / \overline{W} Low to \overline{DS} Low (Write)	tRLSL	80	-	50	-	30	-	30	-	ns
23	Clock Low to Data Out Valid (Write)	tCLDO	-	62	-	50	-	50	-	30	ns
25 ²	\overline{AS} , \overline{DS} High to Data Out Invalid (Write)	tSHDOI	40	-	30	-	20	-	15	-	ns
26 ²	Data Out Valid to \overline{DS} Low (Write)	tDOSL	40	-	30	-	20	-	15	-	ns
27 ⁵	Data in to Clock Low (Setup Time on Read)	tDICL	10	-	10	-	10	-	5	-	ns
28 ²	\overline{AS} , \overline{DS} High to DTACK High (Asynchronous Hold)	tSHDAH	0	240	0	190	0	150	0	110	ns
29	(\overline{AS} , \overline{DS} High to Data-In Invalid (Hold Time on Read)	tSHDII	0	-	0	-	0	-	0	-	ns

* : 68HC000 only

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (3/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, T_a = 0~70°C; See Figure 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
30	\overline{AS} , \overline{DS} High to $\overline{BE\overline{RR}}$ High	tSHBEH	0	–	0	–	0	–	0	–	ns
312.5	\overline{DTACK} Low to Data In (Setup Time)	tDALDI	–	90	–	65	–	50	–	50	ns
32	\overline{HALT} and \overline{RESET} Input Transition	tRHr, f	0	200	0	200	0	200	–	150	ns
33	Clock High to \overline{BG} Low	tCHGL	–	62	–	50	–	40	0	30	ns
34	Clock High to \overline{BG} Low	tCHGH	–	62	–	50	–	40	0	30	ns
35	\overline{BR} Low to \overline{BG} Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36 ⁷	\overline{BR} High to \overline{BG} Low	tBRHGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	\overline{BGACK} Low to \overline{BG} Low	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37A ⁸	\overline{BGACK} Low to \overline{BG} Low	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	10	1.5 Clocks	ns
38	\overline{BG} Width High	tGLZ	–	80	–	70	–	60	–	50	ns
39	\overline{BG} Width High	tGH	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
40	Clock Low to \overline{VMA} Low	tCLVML	–	70	–	70	–	70	–	50	ns
41	Clock Low to E Transition	tCLET	–	55	–	45	–	35	–	35	ns
42	E Output Rise and Fall Time	tEr, f	–	15	–	15	–	15	–	15	ns
43	\overline{VMA} Low to E High	tVMLEH	200	–	150	–	90	–	80	–	ns
44	\overline{AS} , \overline{DS} High to \overline{VPA} High	tSHVPH	0	120	0	90	0	70	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	tELCAI	30	–	10	–	10	–	10	–	ns

* : 68HC000 only

8.5 AC ELECTRICAL SPECIFICATIONS – READ AND WRITE CYCLES (4/4)

(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.3 and 8.4)

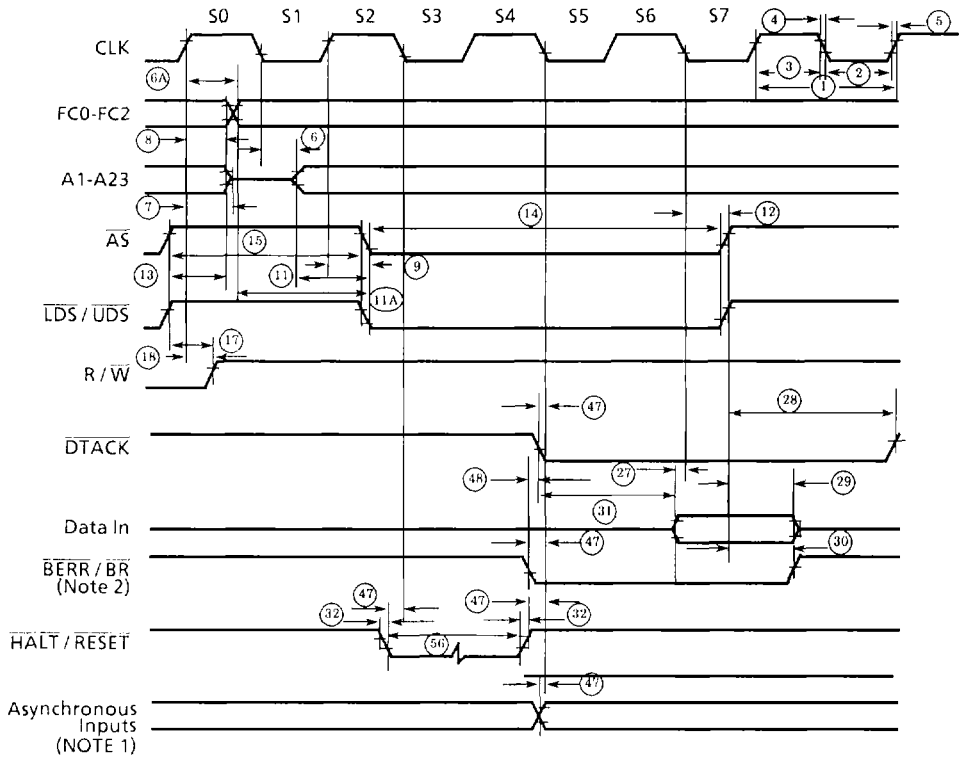
Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		+16.67MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
46	\overline{BGACK} Width Low	tGAL	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
475	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	5	–	ns
482.3	\overline{BERR} Low to \overline{DTACK} Low	tBELDAL	20	–	20	–	20	–	10	–	ns
499	\overline{AS} , \overline{DS} High to E Low	tSHEL	–70	70	–55	55	–45	45	–35	35	ns
50	E Width High	tEH	450	–	350	–	280	–	220	–	ns
51	E Width High	tEL	700	–	550	–	440	–	340	–	ns
53	Clock High to Data Out Invalid	tCHDOI	0	–	0	–	0	–	0	–	ns
54	E Low to Data Out Invalid	tELDOI	30	–	20	–	15	–	10	–	ns
55	R/ \overline{W} to Data Bus Driven	tRLDBD	30	–	20	–	10	–	0	–	ns
564	\overline{HALT} / \overline{RESET} Pulse Width	tHRPW	10	–	10	–	10	–	10	–	Clk. Per.
57	\overline{BGACK} High to Control Bus Driven	tGASD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.
587	\overline{BG} High to Control Bus Driven	tRHSD	1.5	–	1.5	–	1.5	–	1.5	–	Clk. Per.

* : 68HC000 only

Note :

- For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.
- Actual value depends on period.
- If #47 is satisfied for both \overline{DTACK} and \overline{BERR} , #48 may be 0 nanoseconds.
- For powder up, the MPU must be held in \overline{RESET} state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
- If the asynchronous setup time (#47) requirements are satisfied, the \overline{DTACK} low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in clock-low setup time (#27) for the following cycle.
- When \overline{AS} and R/ \overline{W} are equally loaded ($\pm 20\%$), subtract 10 nanoseconds from the values given in these columns.
- The processor will negate \overline{BG} and begin driving the bus again if external arbitration logic negates \overline{BR} before asserting \overline{BGACK} .
- The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, \overline{BG} may be reasserted.
- The falling edge of S6 triggers both the negation of the strobes (\overline{AS} and \overline{DS}) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

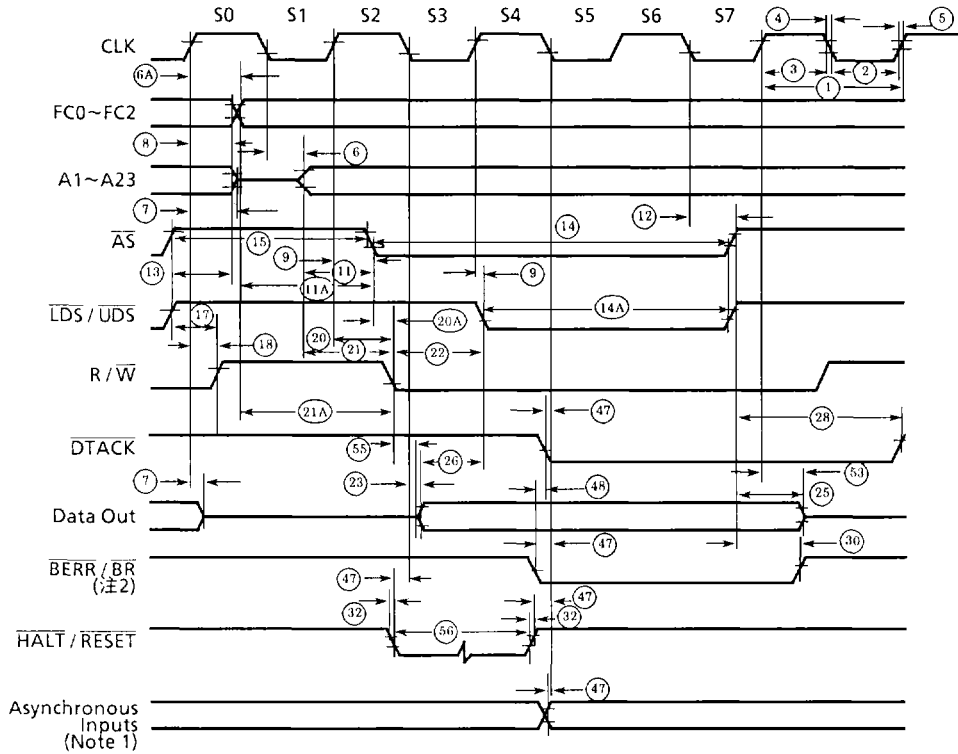


Note :

1. Setup time for the asynchronous inputs $\overline{IPL0} \sim \overline{IPL2}$, and $\overline{VP\bar{A}}$ guarantees their recognition at the next falling edge of the clock.
2. \overline{BR} need fall at this time only in order to insure being recognized at the end of this bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 8.3 Read Cycle Timing Diagram

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note:

1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted.
The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt 2.0 volts.
2. Because of loading variation, R/W may be valid after AS even through both are initiated by the rising edge of S2 (Specification 20A).

Figure 8.4 Write Cycle Timing Diagram

8.6 AC ELECTRICAL SPECIFICATIONS – TMP68HC000 TO 6800 PERIPHERAL

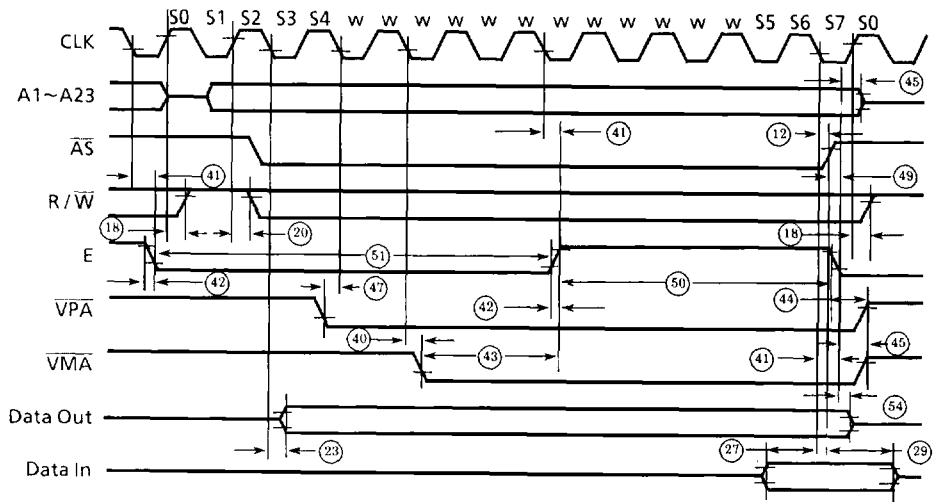
(V_{CC} = 5.0V ± 5%, GND = 0V, Ta = 0~70°C; See Figure 8.5 and 8.6)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
12 ¹	Clock Low to \overline{AS} , \overline{DS} High	tCLSH	-	62	-	50	-	40	3	30	ns
18 ¹	Clock High to R / \overline{W} High	tCHRH	0	55	0	45	0	40	0	30	ns
20 ¹	Clock High to R / \overline{W} Low (Write)	tCHRL	0	55	0	45	0	40	0	30	ns
23	Clock Low to Data Out Valid (Write)	tCLDO	-	62	-	50	-	50	-	30	ns
27	Data In to Clock Low (Setup Time on Read)	tDICL	10	-	10	-	10	-	5	-	ns
29	\overline{AS} , \overline{DS} High to Data in Invalid (Hold Time on Read)	tSHDII	0	-	0	-	0	-	0	-	ns
40	Clock Low to \overline{VMA} Low	tCLVML	-	70	-	70	-	70	-	50	ns
41	Clock Low to E Transition	tCLET	-	55	-	45	-	35	-	35	ns
42	E Output Rise and Fall Time	tEr, f	-	15	-	15	-	15	-	15	ns
43	\overline{VMA} Low to E High	tVMLEH	200	-	150	-	90	-	80	-	ns
44	\overline{AS} , \overline{DS} High to \overline{VPA} High	tSHVPH	0	120	0	90	0	70	0	50	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	tELCAI	30	-	10	-	10	-	10	-	ns
47	Asynchronous Input Setup Time	tASI	10	-	10	-	10	-	5	-	ns
49 ²	\overline{AS} , \overline{DS} High to E Low	tSHEL	-70	70	-55	55	-45	45	-35	35	ns
50	E Width High	tEH	450	-	350	-	280	-	220	-	ns
51	E Width Low	tEL	700	-	550	-	440	-	340	-	ns
54	E Low to Data Out Invalid	tELDOI	30	-	20	-	15	-	10	-	ns

Note 1: For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

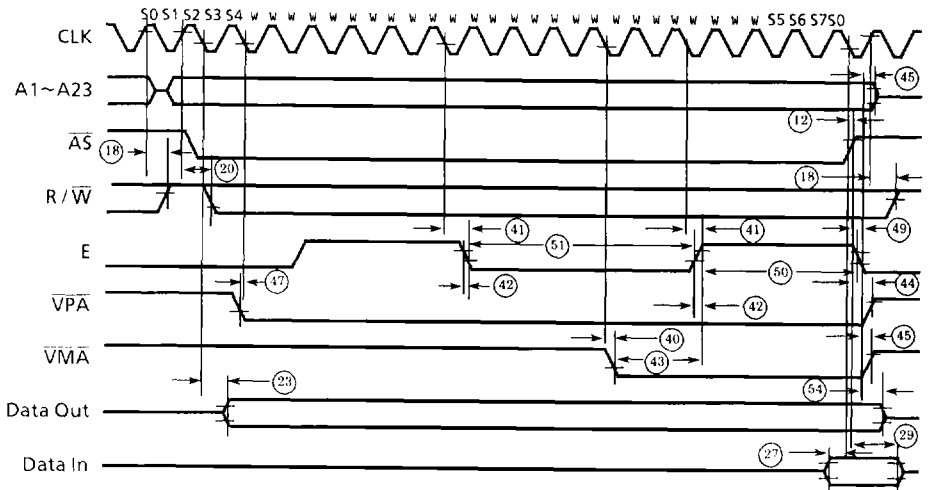
2: The falling edge of S6 triggers both the negation of the strobes (\overline{AS} and \overline{DS}) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and falling edge of the E clock.

*: 68HC000 only



Note : This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the best case possibly attainable.

Figure 8.5 TMP68000 to 6800 Peripheral Timing Diagram – Best Case



Note : This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the worst case possibly attainable.

Figure 8.6 TMP68000 to 6800 Peripheral Timing Diagram – Worst Case

8.7 AC ELECTRICAL SPECIFICATIONS – BUS ARBITRATION

(V_{CC} = 5.0V ± 5%, GND = 0V, T_a = 0~70°C; See Figure 8.7)

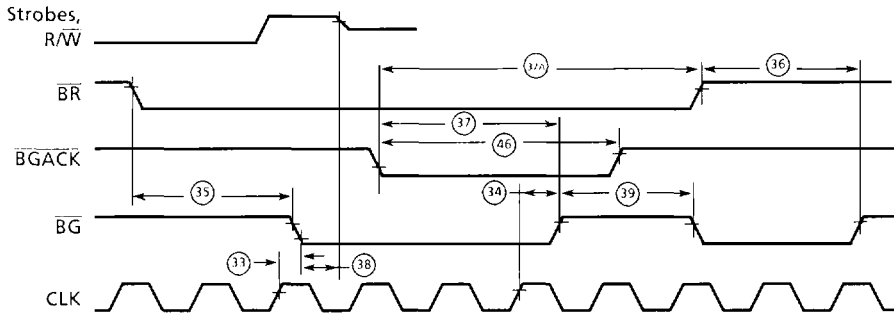
Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		*16.67MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance	tCHADZ	-	80	-	70	-	60	-	50	ns
16	Clock High to Control Bus High Impedance	tCHCZ	-	80	-	70	-	60	-	50	ns
33	Clock High to $\overline{\text{BG}}$ Low	tCHGL	-	62	-	50	-	40	0	30	ns
34	Clock High to $\overline{\text{BG}}$ High	tCHGH	-	62	-	50	-	40	0	30	ns
35	$\overline{\text{BR}}$ Low to $\overline{\text{BG}}$ Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
36 ¹	$\overline{\text{BR}}$ High to $\overline{\text{BG}}$ High	tBKHGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37	$\overline{\text{BGACK}}$ Low to $\overline{\text{BG}}$ High	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per.
37A ²	$\overline{\text{BGACK}}$ Low to $\overline{\text{BR}}$ High	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	10	1.5 Clocks	ns
38	$\overline{\text{BG}}$ Low to Control, Address, Data Bus High Impedance ($\overline{\text{AS}}$ High)	tGLZ	-	80	-	70	-	60	-	50	ns
39	$\overline{\text{BG}}$ Width High	tGH	1.5	-	1.5	-	1.5	-	1.5	-	Clk. Per.
46	$\overline{\text{BGACK}}$ Width Low	tGAL	1.5	-	1.5	-	1.5	-	1.5	-	Clk. Per.
47	Asynchronous Input Setup Time	tASI	10	-	10	-	10	-	5	-	ns
57	$\overline{\text{BGACK}}$ High to Control Bus Driven	tGABD	1.5	-	1.5	-	1.5	-	1.5	-	Clk. Per.
58 ¹	$\overline{\text{BG}}$ High to Control Bus Driven	tGHBD	1.5	-	1.5	-	1.5	-	1.5	-	Clk. Per.

Note: 1. The processor will negate $\overline{\text{BG}}$ and begin driving the bus again if external arbitration logic negates $\overline{\text{BR}}$ before asserting $\overline{\text{BGACK}}$.

2. The minimum value must to guarantee proper operation. If the maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted.

*: 68HC000 only

The waveforms shown in Figures 8.9, 8.10, and 8.11 should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note : Setup time to the clock (#47) for the asynchronous inputs \overline{BERR} , \overline{BGACK} , \overline{BR} , \overline{DTACK} , $IPL0 \sim IPL2$ and VPA guarantees their recognition at the next falling edge of the clock.

Figure 8.7 Bus Arbitration Diagram