

# M5M44256BP, J, L, VP, RV-7, -8, -10

**FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM**

## DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of triple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the  $\overline{RAS}$ -only refresh mode, the hidden refresh mode and  $\overline{CAS}$  before  $\overline{RAS}$  refresh mode are available.

## FEATURES

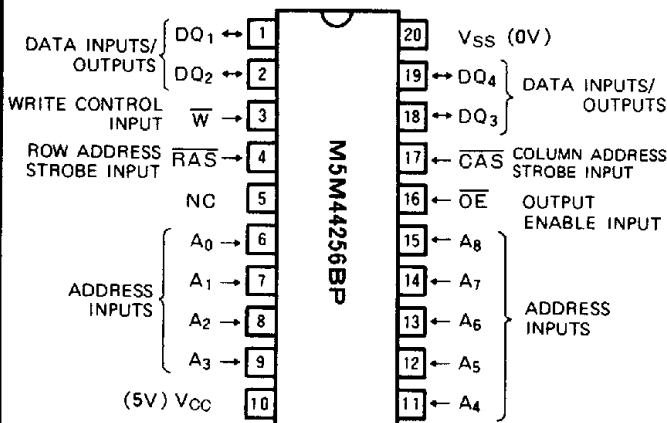
Type name	$\overline{RAS}$ access time (max ns)	$\overline{CAS}$ access time (max ns)	Address access time (max ns)	$\overline{OE}$ access time (max. ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M44256B-7	70	20	35	20	140	230
M5M44256B-8	80	20	40	20	160	200
M5M44256B-10	100	25	50	25	190	175

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP, 24 pin TSOP
- Single 5V±10% supply
- Low stand-by power dissipation  
2.75mW (max) . . . . . CMOS Input level
- Low operating power dissipation  
M5M44256BP, J, L, VP, RV-7 . . . 440mW (max)  
M5M44256BP, J, L, VP, RV-8 . . . 385mW (max)  
M5M44256BP, J, L, VP, RV-10 . . 330mW (max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and  $\overline{OE}$  control output buffer impedance
- Read-Modify-write,  $\overline{RAS}$ -only refresh, Fast-page mode capabilities
- $\overline{CAS}$  before  $\overline{RAS}$  refresh mode capability
- $\overline{CAS}$  controlled output allows hidden refresh
- Wide  $\overline{RAS}$  Low pulse width for  
Fast page mode . . . . . 50µs (max)

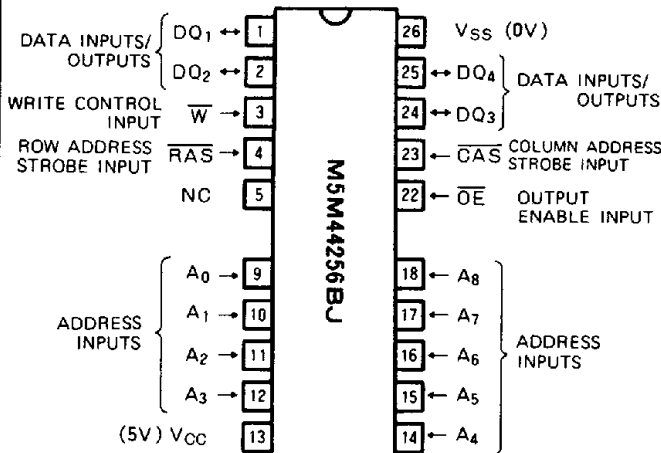
## APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

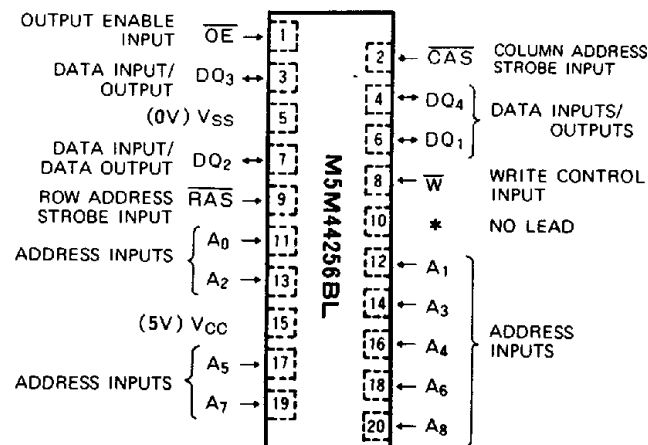
## PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)

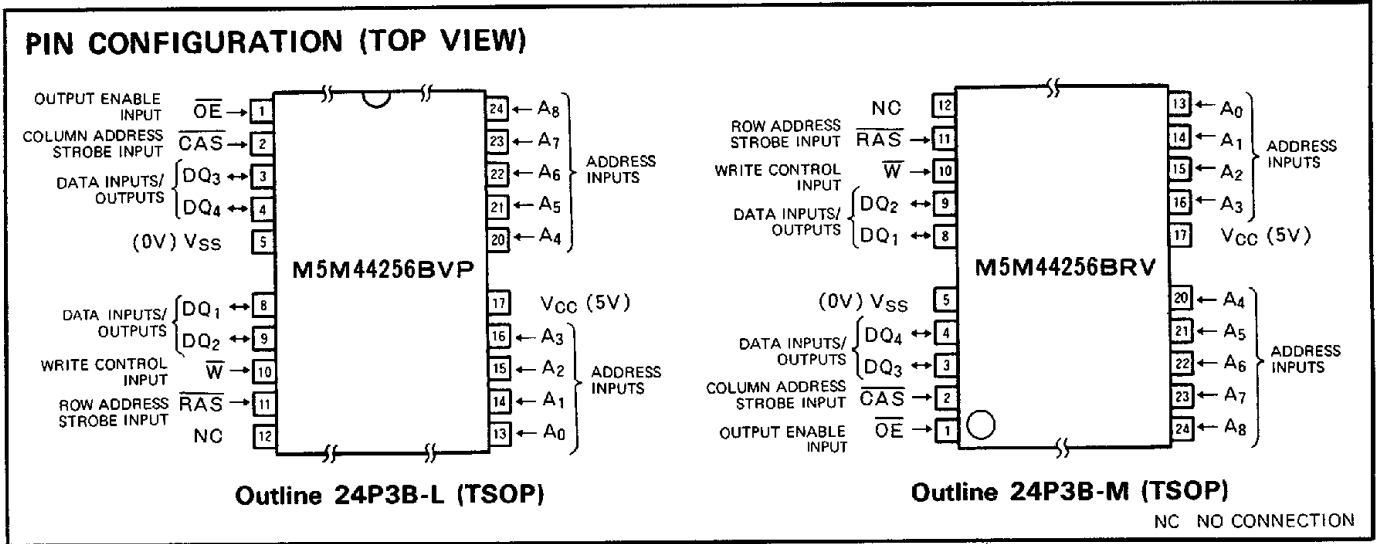


Outline 20P5L-A(ZIP)

NC NO CONNECTION

# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM



### FUNCTION

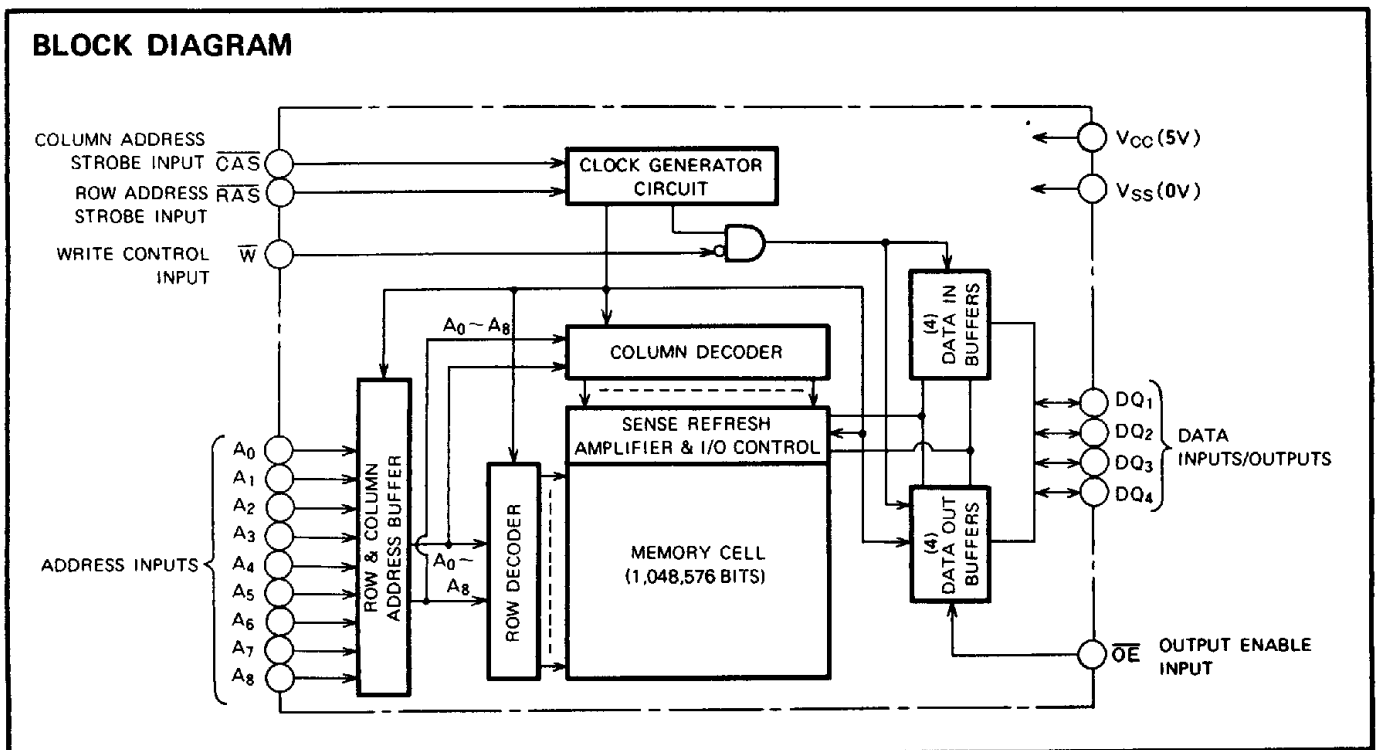
The M5M44256BP, J, L, VP, RV provide, in addition to normal read, write, and read-modify-write operations, a

number of other functions, e.g., fast page mode,  $\overline{RAS}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, APD applied, OPN open



**M5M44256BP, J, L, VP, RV-7, -8, -10****FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM****ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage	With respect to V <sub>SS</sub>	-1 ~ 7	V
V <sub>I</sub>	Input voltage		-1 ~ 7	V
V <sub>O</sub>	Output voltage		-1 ~ 7	V
I <sub>O</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	1000	mW
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

**RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = 0 ~ 70°C, unless otherwise noted) (Note 1)**

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>SS</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.4		6.5	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-1.0		0.8	V

Note 1 All voltage values are with respect to V<sub>SS</sub>**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0 ~ 70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, unless otherwise noted) (Note 2)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5mA	2.4		V <sub>CC</sub>	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2mA	0		0.4	V
I <sub>OZ</sub>	Off state output current	Q floating 0V ≤ V <sub>OUT</sub> ≤ 5.5V	-10		10	μA
I <sub>I</sub>	Input current	0V ≤ V <sub>IN</sub> ≤ 6.5V, Other inputs pins = 0V	-10		10	μA
I <sub>CC1</sub> (AV)	Average supply current from V <sub>CC</sub> , operating (Note 3, 4)	M5M44256B-7 M5M44256B-8 M5M44256B-10 R <sub>AS</sub> , C <sub>AS</sub> cycling t <sub>RC</sub> = t <sub>WC</sub> = min, output open			80	mA
					70	
					60	
I <sub>CC2</sub> (AV)	Average supply current from V <sub>CC</sub> , stand-by (Note 6)	R <sub>AS</sub> = C <sub>AS</sub> = V <sub>IH</sub> , output open R <sub>AS</sub> = C <sub>AS</sub> = 0E ≥ V <sub>CC</sub> - 0.5V, output open			2	mA
					0.5	
I <sub>CC3</sub> (AV)	Average supply current from V <sub>CC</sub> , refreshing (Note 3)	M5M44256B-7 M5M44256B-8 M5M44256B-10 R <sub>AS</sub> cycling, C <sub>AS</sub> = V <sub>IH</sub> t <sub>RC</sub> = min, output open			80	mA
					70	
					60	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>CC</sub> , Fast-Page-Mode (Note 3, 4)	M5M44256B-7 M5M44256B-8 M5M44256B-10 R <sub>AS</sub> = V <sub>IL</sub> , C <sub>AS</sub> cycling t <sub>PC</sub> = min, output open			70	mA
					60	
					50	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>CC</sub> , C <sub>AS</sub> before R <sub>AS</sub> refresh mode (Note 3)	M5M44256B-7 M5M44256B-8 M5M44256B-10 C <sub>AS</sub> before R <sub>AS</sub> refresh cycling t <sub>RC</sub> = min, output open			80	mA
					70	
					60	

Note 2. Current flowing into an IC is positive, out is negative

3 I<sub>CC1</sub>(AV), I<sub>CC3</sub>(AV), I<sub>CC4</sub>(AV) and I<sub>CC6</sub>(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate4 I<sub>CC1</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on output loading. Specified values are obtained with the output open**CAPACITANCE (T<sub>a</sub> = 0 ~ 70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I(A)</sub>	Input capacitance, address inputs (Note 5)	V <sub>I</sub> = V <sub>SS</sub> f = 1MHz V <sub>I</sub> = 25mVrms			5	pF
C <sub>I(0E)</sub>	Input capacitance, 0E input				7	pF
C <sub>I(W)</sub>	Input capacitance, write control input				7	pF
C <sub>I(RAS)</sub>	Input capacitance, RAS input				7	pF
C <sub>I(CAS)</sub>	Input capacitance, CAS input				7	pF
C <sub>I/O</sub>	Input/Output capacitance, data ports				7	pF

Note 5 C<sub>I(A)</sub> of ZIP is 6pF (max).

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### SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted) (Note 6)

Symbol	Parameter	Limits						Unit
		M5M4256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>CAC</sub>	Access time from $\overline{\text{CAS}}$ (Note 7, 8)		20		20		25	ns
t <sub>RAC</sub>	Access time from $\overline{\text{RAS}}$ (Note 7, 9)		70		80		100	ns
t <sub>CAA</sub>	Column Address access time (Note 7, 10)		35		40		50	ns
t <sub>CPA</sub>	Access time from $\overline{\text{CAS}}$ precharge (Note 7, 11)		40		45		55	ns
t <sub>OEa</sub>	Access time from $\overline{\text{OE}}$ (Note 7)		20		20		25	ns
t <sub>CLZ</sub>	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		ns
t <sub>OFF</sub>	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	20	0	20	0	25	ns
t <sub>dis(OE)</sub>	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	20	0	20	0	25	ns

- Note 6: An initial pause of 500μs is required after power-up followed by any 8  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}/\overline{\text{CAS}}$  cycles before proper device operation is achieved. Note that  $\overline{\text{RAS}}$  may be cycled during the initial pause. And any 8  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}/\overline{\text{CAS}}$  cycles are required after prolonged periods of  $\overline{\text{RAS}}$  inactivity before proper device operation is achieved.
- 7: Measured with a load circuit equivalent to 2TTL loads and 100pF.
- 8: Assume that  $t_{\text{RCD(max)}} \leq t_{\text{RCD}}$  and  $t_{\text{ASC}} \geq t_{\text{ASC(max)}}$ .
- 9: Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD(max)}}$  and  $t_{\text{RAD}} \leq t_{\text{RAD(max)}}$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by amount that  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  exceeds the value shown.
- 10: Assume that  $t_{\text{RAD}} \geq t_{\text{RAD(max)}}$  and  $t_{\text{ASC}} \leq t_{\text{ASC(max)}}$ .
- 11: Assume that  $t_{\text{CP}} \leq t_{\text{CP(max)}}$  and  $t_{\text{ASC}} \geq t_{\text{ASC(max)}}$ .
- 12:  $t_{\text{OFF(max)}}$  and  $t_{\text{dis(OE)(max)}}$  define the time at which the output achieves the high impedance state ( $I_{\text{OUT}} \leq \pm 10\mu\text{A}$ ) and are not reference to  $V_{\text{OH(min)}}$  or  $V_{\text{OL(max)}}$ .

### TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles)

(Ta = 0 ~ 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted, See notes 13, 14)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>REF</sub>	Refresh cycle time		8		8		8	ms
t <sub>RP</sub>	$\overline{\text{RAS}}$ high pulse width	60		70		80		ns
t <sub>RCD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note 15)	20	50	25	60	25	75	ns
t <sub>CRP</sub>	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low (Note 16)	10		10		10		ns
t <sub>CPN</sub>	$\overline{\text{CAS}}$ high pulse width	10		10		10		ns
t <sub>RAD</sub>	Column address delay time from $\overline{\text{RAS}}$ low (Note 17)	15	35	20	40	20	50	ns
t <sub>ASR</sub>	Row address setup time before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>ASC</sub>	Column address setup time before $\overline{\text{CAS}}$ low (Note 18)	0	10	0	15	0	20	ns
t <sub>RAH</sub>	Row address hold time after $\overline{\text{RAS}}$ low	10		15		15		ns
t <sub>CAH</sub>	Column address hold time after $\overline{\text{CAS}}$ low	15		20		20		ns
t <sub>T</sub>	Transition time (Note 19)	3	50	3	50	3	50	ns

- Note 13: The timing requirements are assumed  $t_{\text{T}} = 5\text{ns}$ .
- 14:  $V_{\text{IH(min)}}$  and  $V_{\text{IL(max)}}$  are reference levels for measuring timing of input signals.
- 15:  $t_{\text{RCD(max)}}$  is specified as a reference point only. If  $t_{\text{RCD}}$  is less than  $t_{\text{RCD(max)}}$ , access time is  $t_{\text{RAC}}$ . If  $t_{\text{RCD}}$  is greater than  $t_{\text{RCD(max)}}$ , access time is defined as  $t_{\text{CAC}}$  and  $t_{\text{CAA}}$  as shown in notes 8, 10.
- 16:  $t_{\text{CRP}}$  requirement is applicable for all  $\overline{\text{RAS}}/\overline{\text{CAS}}$  cycles.
- 17:  $t_{\text{RAD(max)}}$  is specified as a reference point only. If  $t_{\text{RAD}} \geq t_{\text{RAD(max)}}$  and  $t_{\text{ASC}} \leq t_{\text{ASC(max)}}$ , access time is controlled exclusively by  $t_{\text{CAA}}$ .
- 18:  $t_{\text{ASC(max)}}$  is specified as a reference point only. If  $t_{\text{RCD}} \geq t_{\text{RCD(max)}}$  and  $t_{\text{ASC}} \geq t_{\text{ASC(max)}}$ , access time is controlled exclusively by  $t_{\text{CAC}}$ .
- 19:  $t_{\text{T}}$  is measured between  $V_{\text{IH(min)}}$  and  $V_{\text{IL(max)}}$ .

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### Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>RC</sub>	Read cycle time	140		160		190		ns
t <sub>RAS</sub>	$\overline{RAS}$ low pulse width	70	10000	80	10000	100	10000	ns
t <sub>CAS</sub>	$\overline{CAS}$ low pulse width	20	10000	20	10000	25	10000	ns
t <sub>CSH</sub>	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t <sub>RSH</sub>	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		25		ns
t <sub>RCS</sub>	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
t <sub>RCH</sub>	Read hold time after $\overline{CAS}$ high (Note 20)	0		0		0		ns
t <sub>RRH</sub>	Read hold time after $\overline{RAS}$ high (Note 20)	10		10		10		ns
t <sub>RAL</sub>	Column address to $\overline{RAS}$ setup time	35		40		50		ns
t <sub>RPC</sub>	Precharge to $\overline{CAS}$ active time	0		0		0		ns
t <sub>h(CLOE)</sub>	$\overline{OE}$ hold time after $\overline{CAS}$ low	20		20		25		ns
t <sub>h(RLOE)</sub>	$\overline{OE}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t <sub>DOEL</sub>	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t <sub>OEHD</sub>	Delay time, $\overline{OE}$ high to Data	15		15		20		ns
t <sub>h(OECH)</sub>	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		20		25		ns
t <sub>h(ERH)</sub>	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		20		25		ns

Note 20 Either t<sub>RCH</sub> or t<sub>RRH</sub> must be satisfied for a read cycle

### Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	140		160		190		ns
t <sub>RAS</sub>	$\overline{RAS}$ low pulse width	70	10000	80	10000	100	10000	ns
t <sub>CAS</sub>	$\overline{CAS}$ low pulse width	20	10000	20	10000	25	10000	ns
t <sub>CSH</sub>	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t <sub>RSH</sub>	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		20		25		ns
t <sub>WCS</sub>	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
t <sub>WCH</sub>	Write hold time after $\overline{CAS}$ low	15		15		20		ns
t <sub>OWL</sub>	$\overline{CAS}$ hold time after write low	20		20		25		ns
t <sub>RWL</sub>	$\overline{RAS}$ hold time after write low	20		20		25		ns
t <sub>WP</sub>	Write pulse width	15		15		20		ns
t <sub>DS</sub>	Data setup time	0		0		0		ns
t <sub>DH</sub>	Data hold time after $\overline{CAS}$ low	15		15		20		ns
t <sub>OEHD</sub>	Delay time, $\overline{OE}$ high to data	15		15		20		ns
t <sub>h(WOE)</sub>	$\overline{OE}$ hold time after write low	15		15		20		ns

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### Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>RWC</sub>	Read-write/read-modify-write cycle time (Note 21)	185		205		245		ns
t <sub>RAS</sub>	RAS low pulse width	115	10000	125	10000	155	10000	ns
t <sub>CAS</sub>	CAS low pulse width	65	10000	65	10000	80	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	115		125		155		ns
t <sub>RSH</sub>	RAS hold time after CAS low	65		65		80		ns
t <sub>RCS</sub>	Read setup time before CAS low	0		0		0		ns
t <sub>CWD</sub>	Delay time, CAS low to write low (Note 22)	40		40		50		ns
t <sub>RWD</sub>	Delay time, RAS low to write low (Note 22)	90		100		125		ns
t <sub>CWL</sub>	CAS hold time after write low	20		20		25		ns
t <sub>RWL</sub>	RAS hold time after write low	20		20		25		ns
t <sub>WP</sub>	Write pulse width	15		15		20		ns
t <sub>DS</sub>	Data setup time	0		0		0		ns
t <sub>DH</sub>	Data hold time after write low	15		15		20		ns
t <sub>AWD</sub>	Delay time, address to write low (Note 22)	55		60		75		ns
t <sub>h(CLOE)</sub>	OE hold time after CAS low	20		20		25		ns
t <sub>h(RLOE)</sub>	OE hold time after RAS low	70		80		100		ns
t <sub>DOEL</sub>	Delay time, Data to OE low	0		0		0		ns
t <sub>OEHD</sub>	Delay time, OE high to Data	15		15		20		ns
t <sub>h(WOE)</sub>	OE hold time after write low	15		15		20		ns

Note 21 t<sub>RWC</sub> is specified as t<sub>RWC(min)</sub> = t<sub>RAC(max)</sub> + t<sub>OEHD(min)</sub> + t<sub>RWL(min)</sub> + t<sub>RP(min)</sub> + 4t<sub>T</sub>

22 t<sub>WCS</sub>, t<sub>CWD</sub>, t<sub>RWD</sub> and t<sub>AWD</sub> are specified as reference points only. If t<sub>WCS</sub> ≥ t<sub>WCS(min)</sub> the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t<sub>CWD</sub> ≥ t<sub>CWD(min)</sub>, t<sub>RWD</sub> ≥ t<sub>RWD(min)</sub> and t<sub>AWD</sub> ≥ t<sub>AWD(min)</sub>, the cycle is a read-modify write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until CAS or OE goes back to V<sub>IH</sub>) is indeterminate.

### Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>PC</sub>	Read, Write cycle time	45		50		60		ns
t <sub>RWPC</sub>	Read-write/read-modify-write cycle time	95		100		115		ns
t <sub>RAS</sub>	RAS low pulse width for Read, write cycle	115	50000	130	50000	160	50000	ns
t <sub>CAS</sub>	CAS low pulse width for read cycle	20	10000	20	10000	25	10000	ns
t <sub>CP</sub>	CAS high pulse width (Note 23)	10	25	10	25	10	25	ns
t <sub>RSH</sub>	RAS hold time after CAS low	20		20		25		ns

Note 23 t<sub>CP(max)</sub> is specified as a reference point only. If t<sub>CP(max)</sub> ≤ t<sub>CP</sub>, access time is assumed by t<sub>CAC</sub>.

### CAS before RAS Refresh Cycle (Note 24)

Symbol	Parameter	Limits						Unit
		M5M44256B-7		M5M44256B-8		M5M44256B-10		
		Min	Max	Min	Max	Min	Max	
t <sub>CSR</sub>	CAS setup time for CAS before RAS refresh	10		10		10		ns
t <sub>CHR</sub>	CAS hold time for CAS before RAS refresh	15		15		20		ns
t <sub>RPC</sub>	Precharge to CAS active time	0		0		0		ns

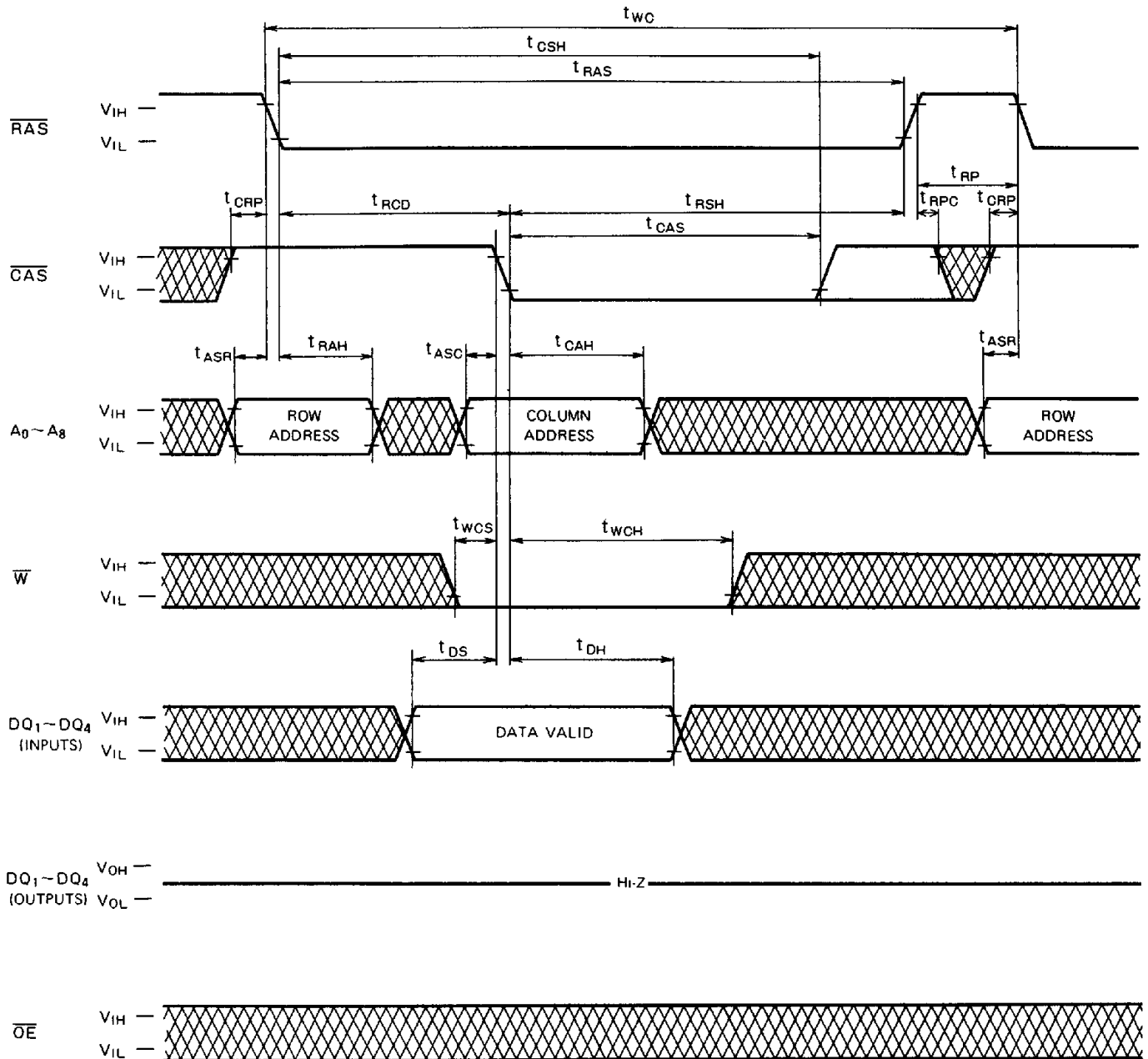
Note 24 Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.



# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

### Write Cycle (Early write)

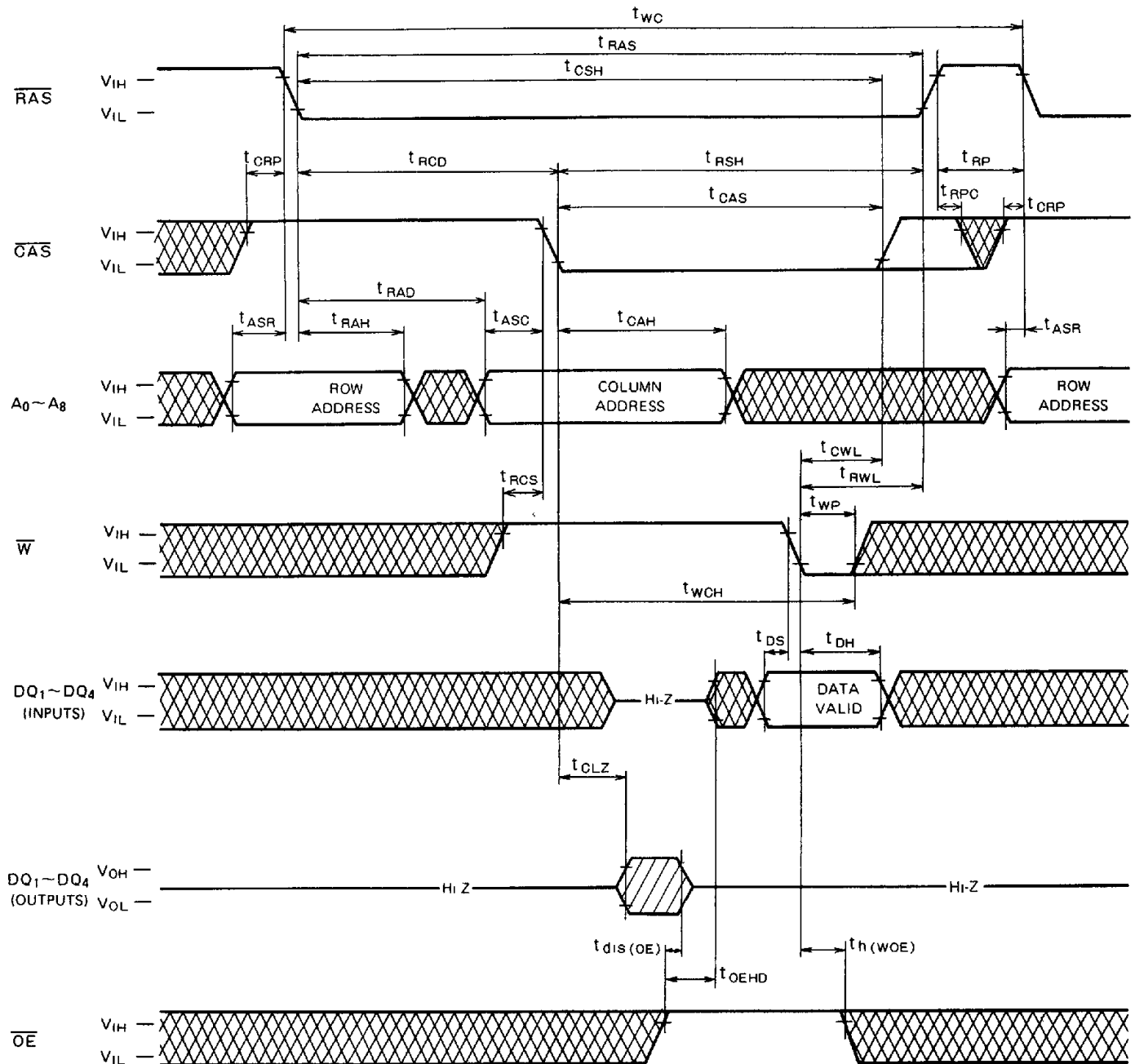




# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

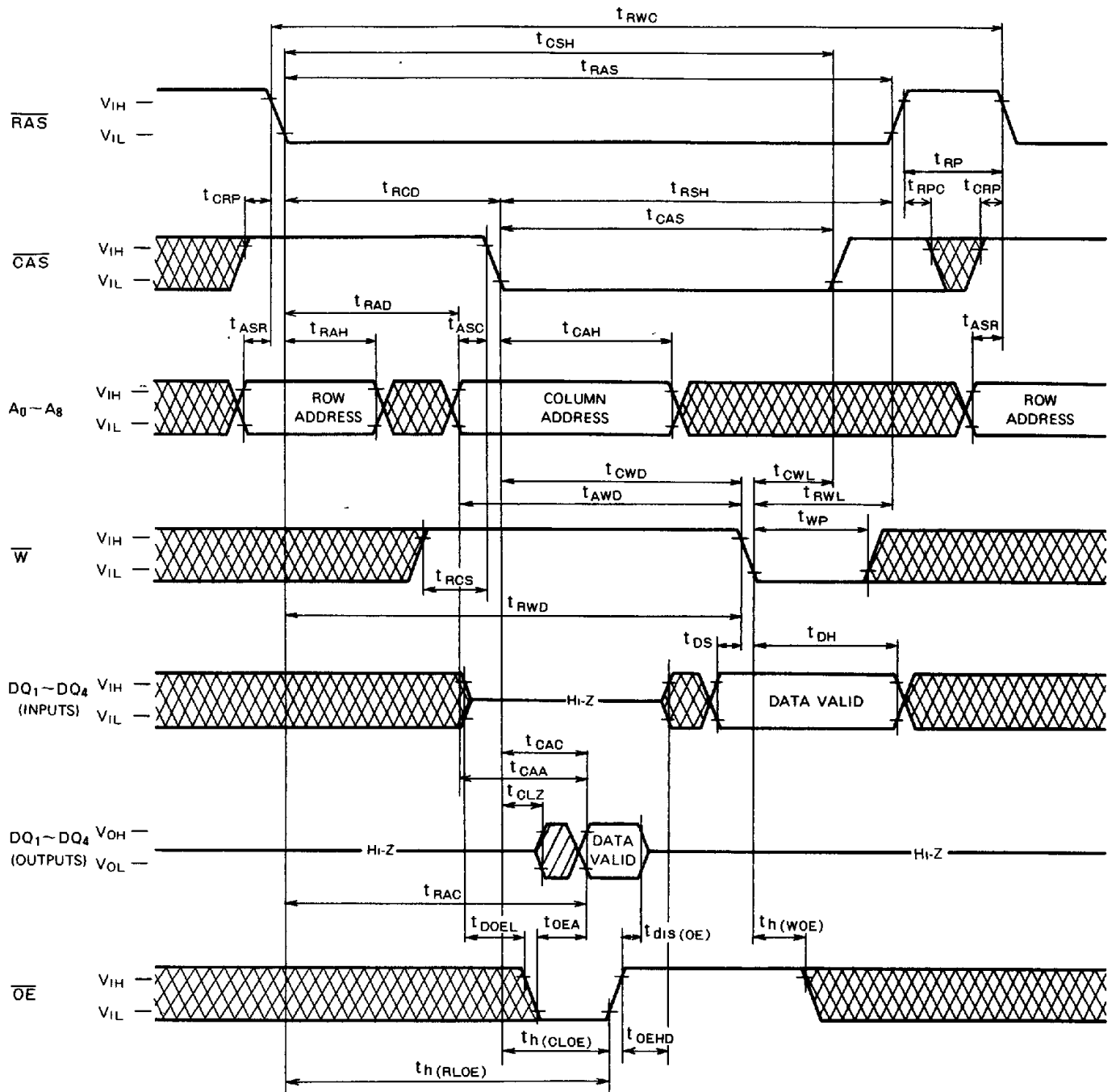
### Write Cycle (Delayed Write)



# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

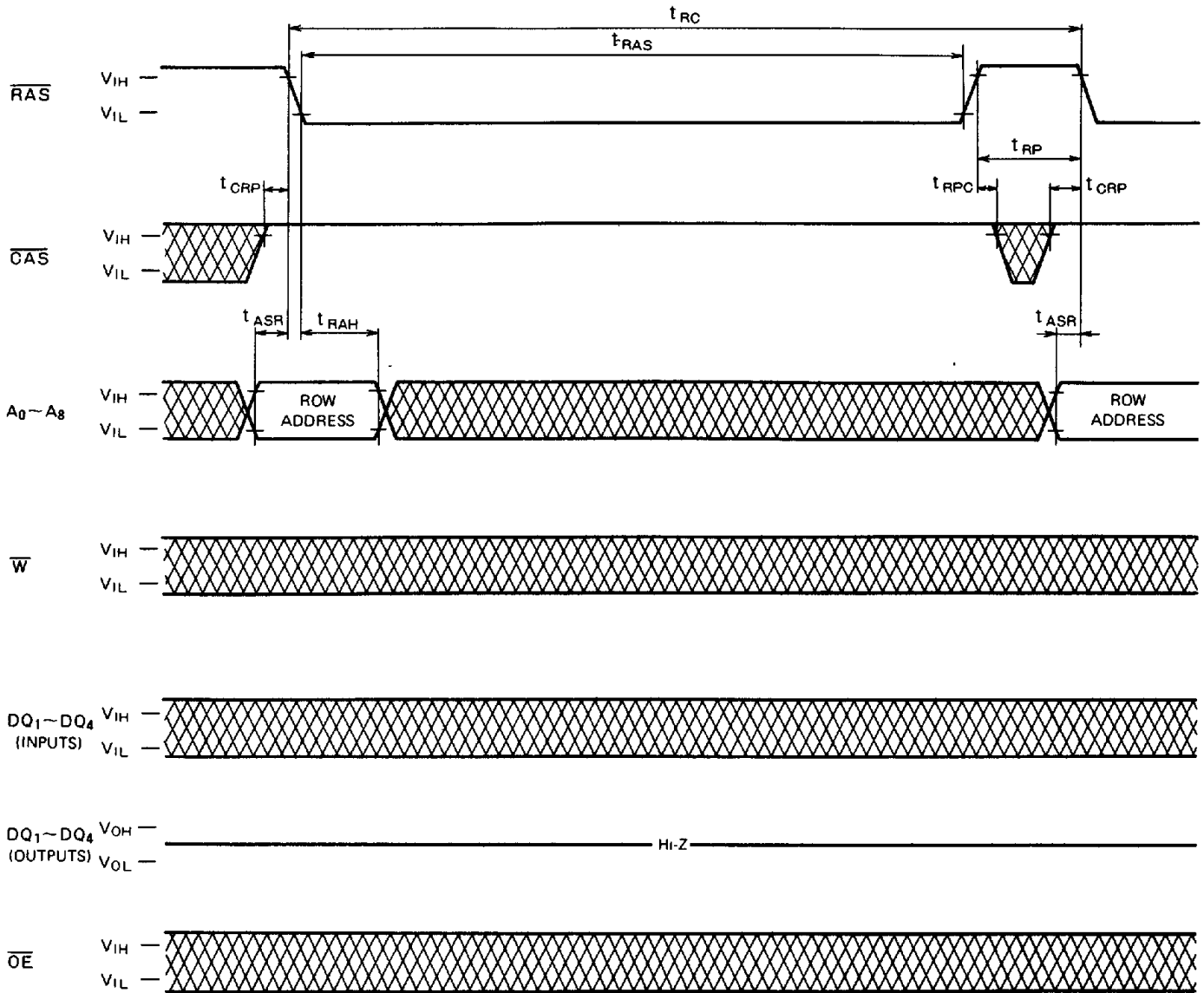
### Read-Write, Read-Modify-Write Cycle



# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT) DYNAMIC RAM

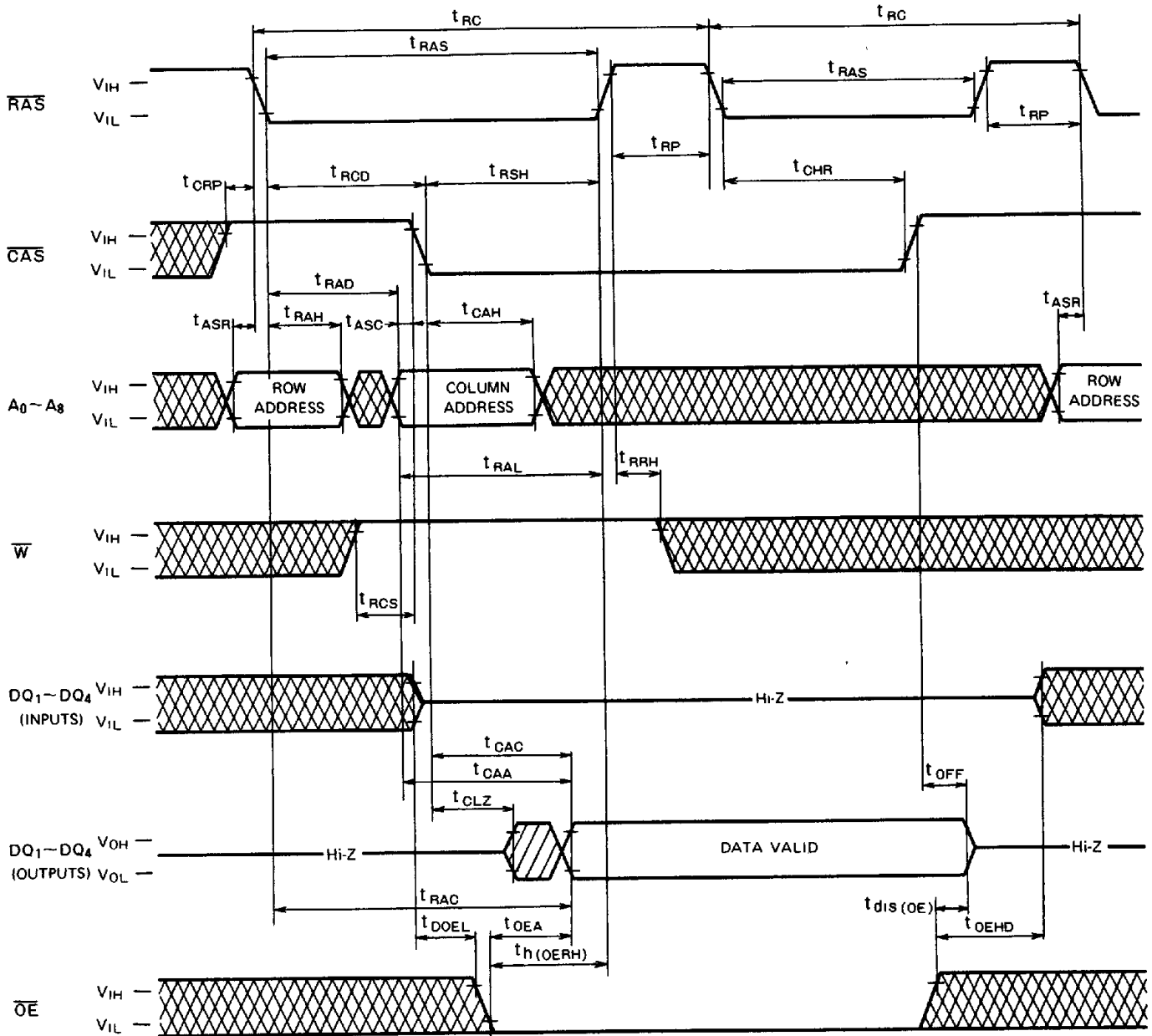
### $\overline{\text{RAS}}$ -only Refresh Cycle



# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

### Hidden Refresh Cycle (Read) (Note 26)

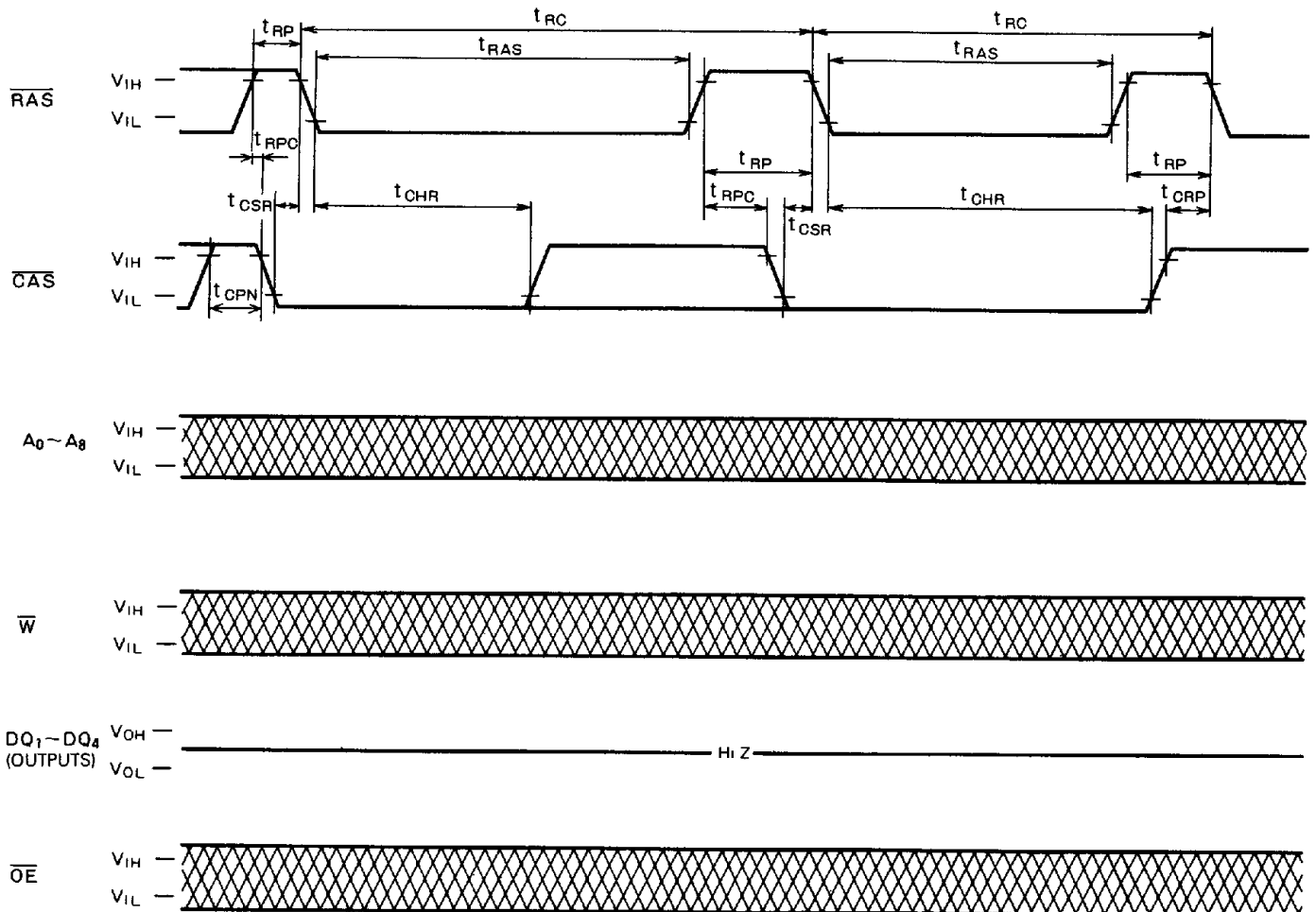


Note 26: Early write, delayed write, read-write or read-modify-write cycle is applicable instead of read cycle  
Timing requirements and output state are the same as that of each cycle shown before

# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT) DYNAMIC RAM

### $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

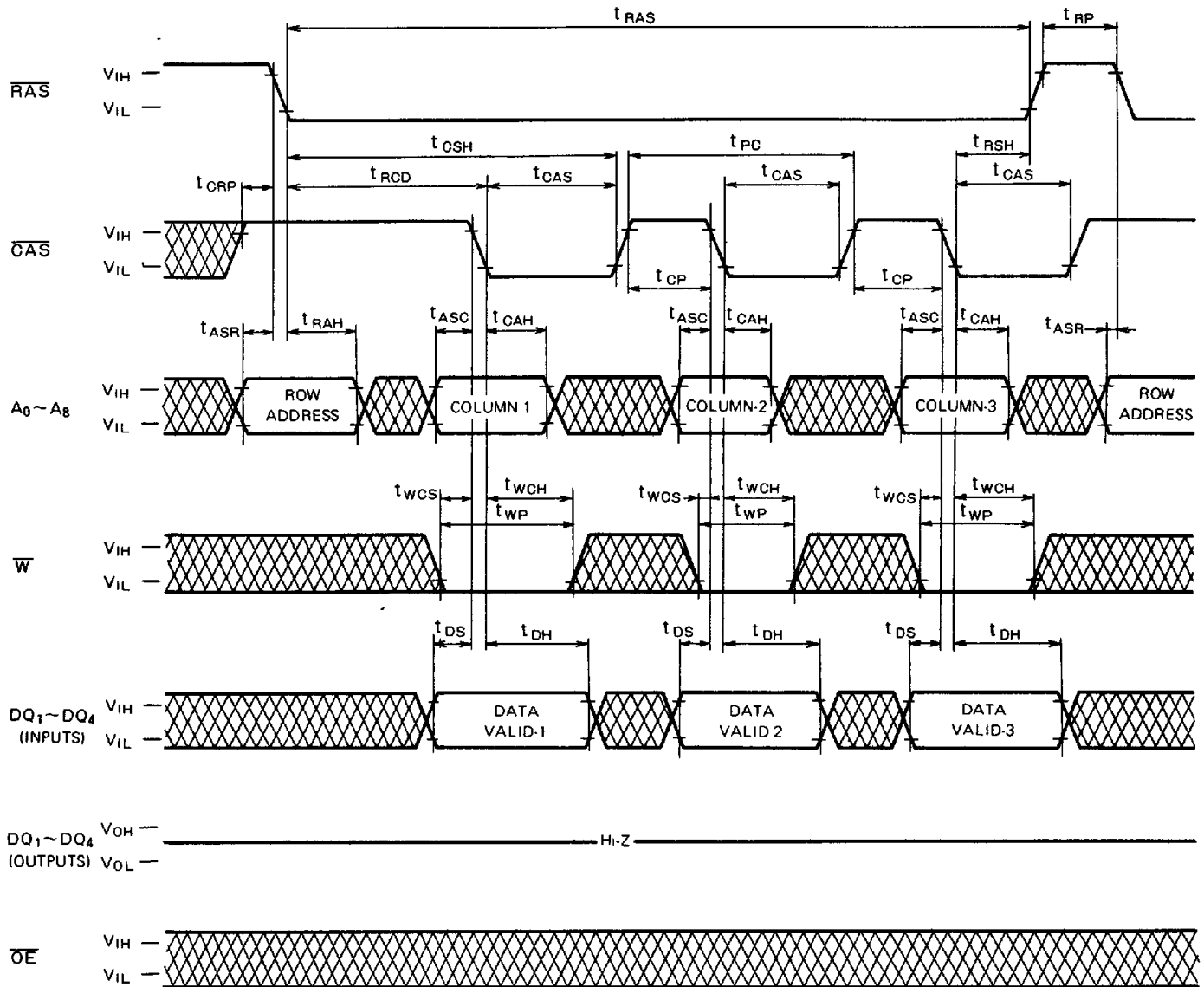




# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

### Fast Page Mode Write Cycle (Early Write)



# M5M44256BP, J, L, VP, RV-7, -8, -10

## FAST PAGE MODE 1048576-BIT(262144-WORD BY 4-BIT) DYNAMIC RAM

### Fast Page Mode Write Cycle (Delayed Write)

