

DM74LS00 Quad 2-Input NAND Gate

General Description

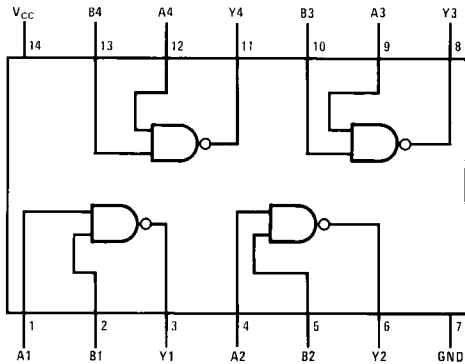
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min		0.35	0.5	V
		I _{OL} = 4 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.36	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{OCH}	Supply Current with Outputs HIGH	V _{CC} = Max		0.8	1.6	mA
I _{OCL}	Supply Current with Outputs LOW	V _{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

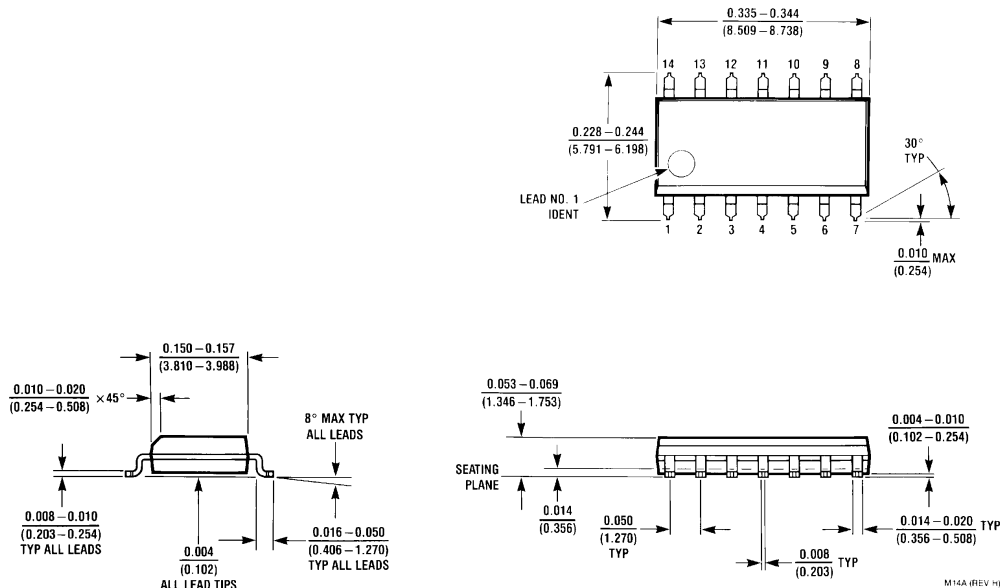
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R _L = 2 kΩ				Units
		C _L = 15 pF		C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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DM7404

Hex Inverting Gates

General Description

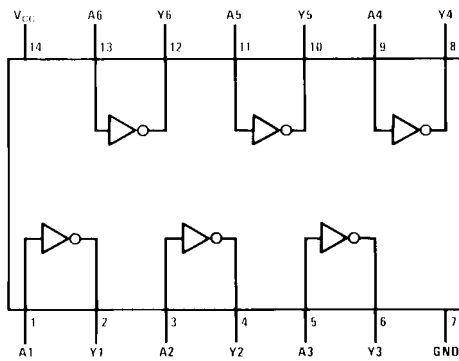
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \bar{A}$$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5\text{V}$			1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4\text{V}$			40	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$			-1.6	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	-18		-55	mA
I_{CCH}	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$		6	12	mA
I_{CCL}	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$		18	33	mA

Note 2: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

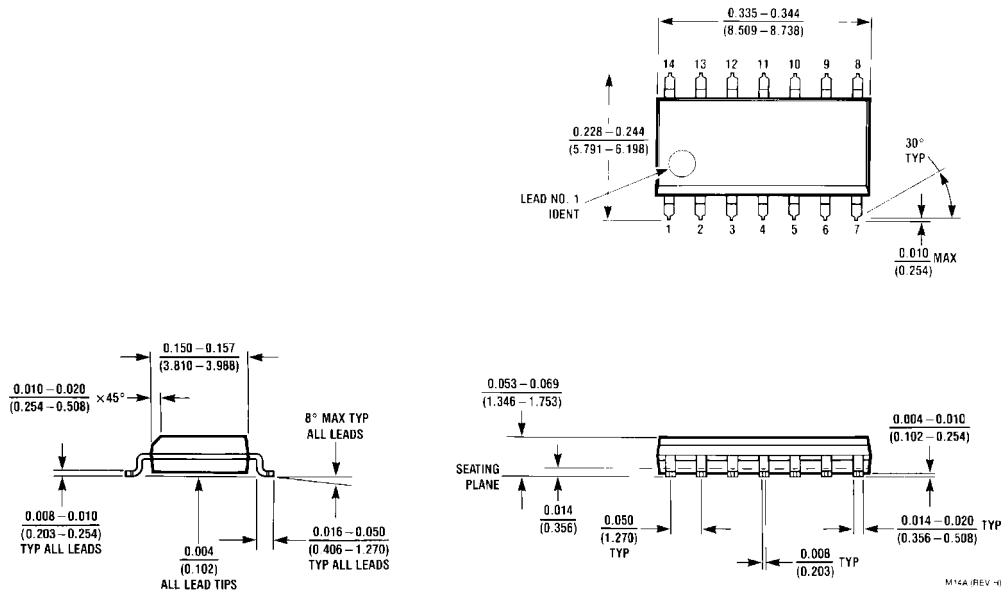
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

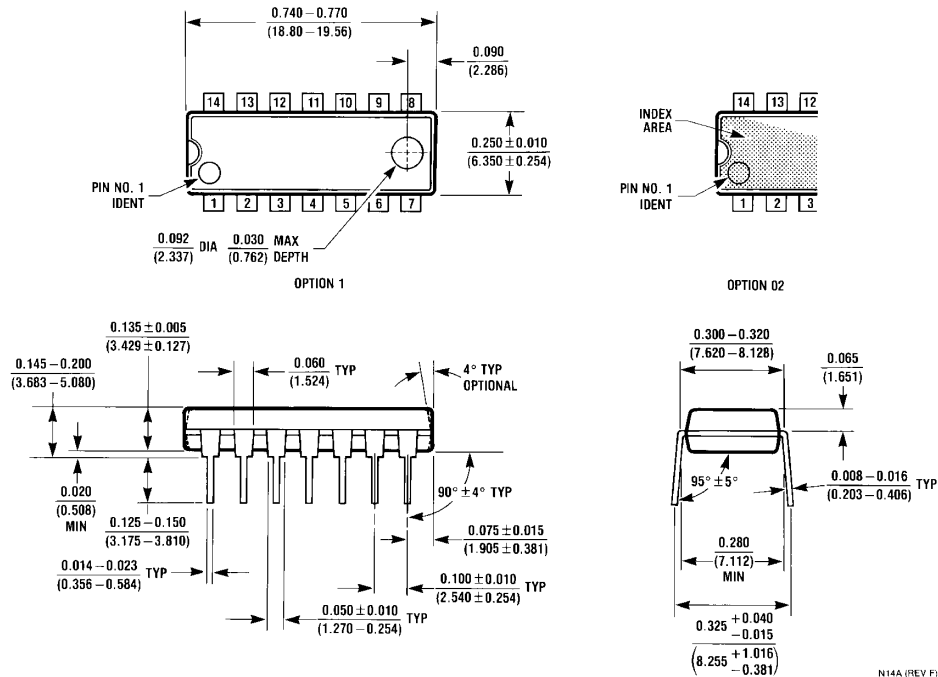
Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

M14A (REV. H)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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DM74LS30

8-Input NAND Gate

General Description

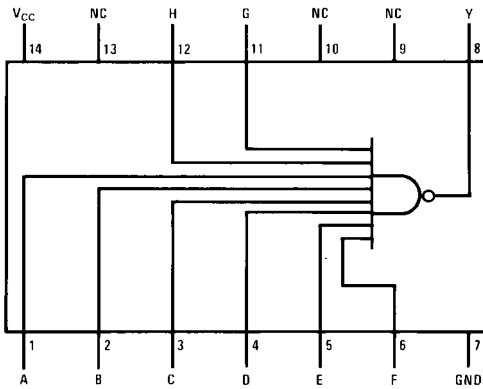
This device contains a single gate which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS30M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS30N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max	2.7	3.4		V
V _{OL}	LOW Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min I _{OL} = 4 mA, V _{CC} = Min		0.35 0.25	0.5 0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CCH}	Supply Current with Outputs HIGH	V _{CC} = Max		0.35	0.5	mA
I _{CCL}	Supply Current with Outputs LOW	V _{CC} = Max		0.6	1.1	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

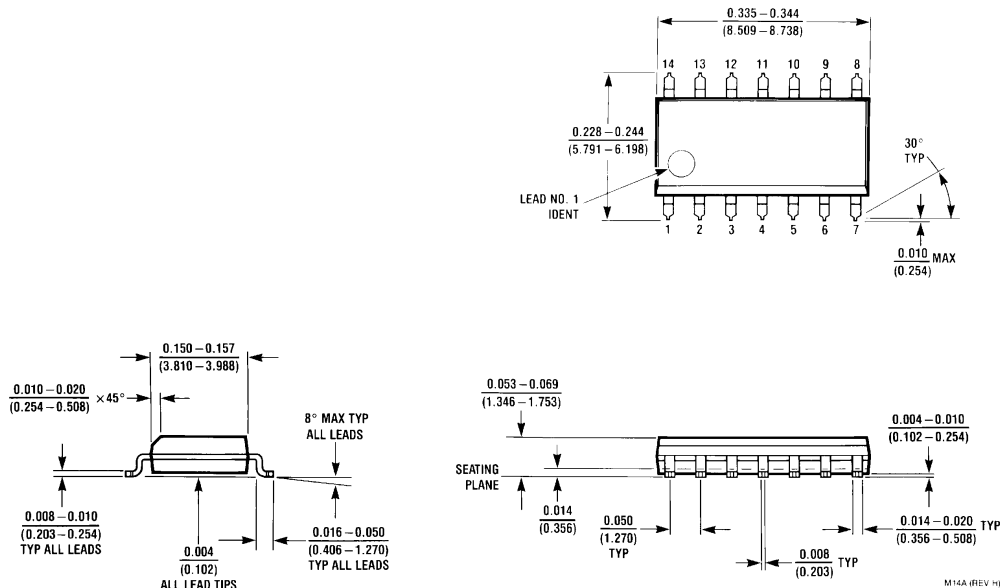
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

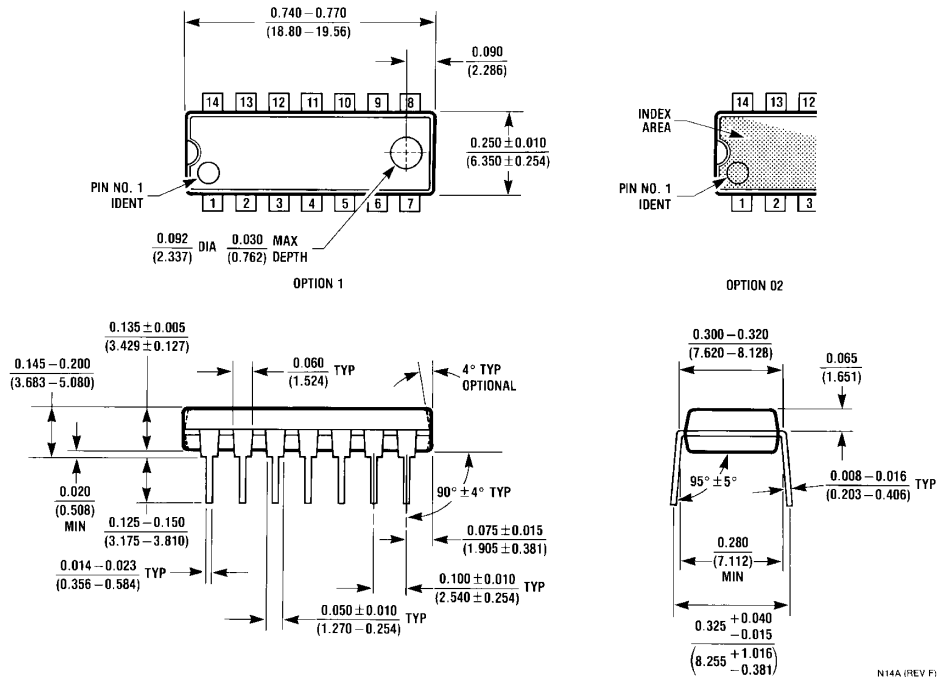
Symbol	Parameter	R _L = 2 kΩ				Units
		C _L = 15 pF		C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	12	5	18	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	4	15	5	20	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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DM74LS161A • DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM74LS161A and DM74LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the DM74LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs LOW, regardless of the levels of clock, load, or enable inputs. The clear function for the DM74LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs LOW after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be HIGH to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. HIGH-to-LOW level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

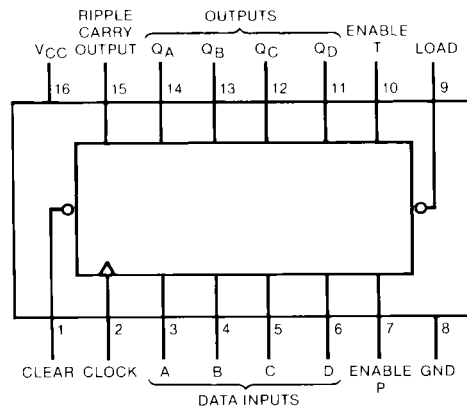
- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

Ordering Code:

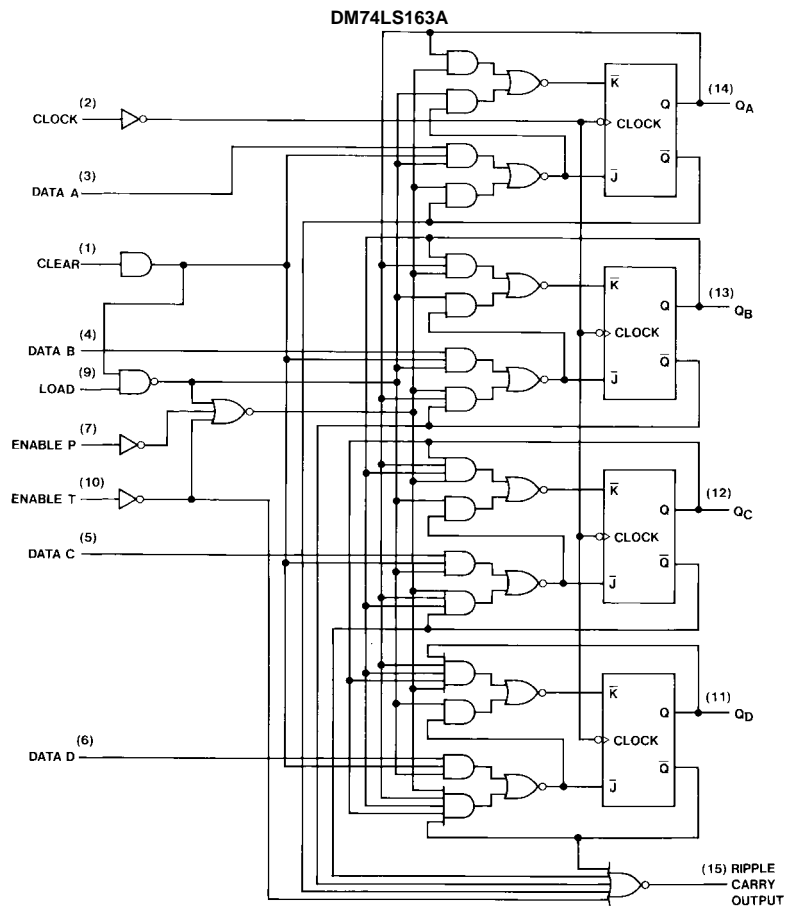
Order Number	Package Number	Package Description
DM74LS161AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS161AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS163AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS163AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



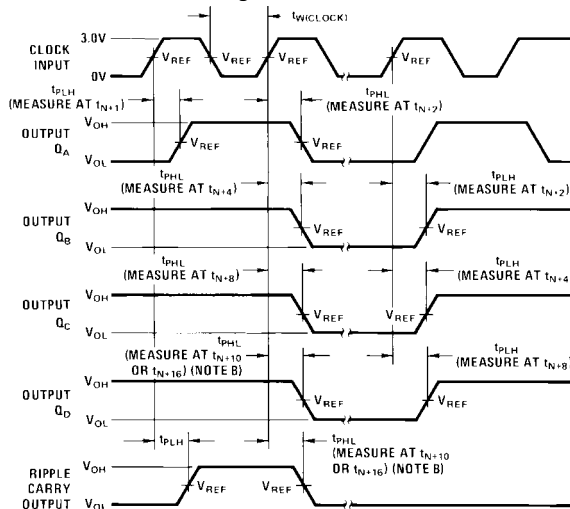
Logic Diagram



The DM74LS161A is similar, however, the clear buffer is connected directly to the flip-flops.

Parameter Measurement Information

Switching Time Waveforms



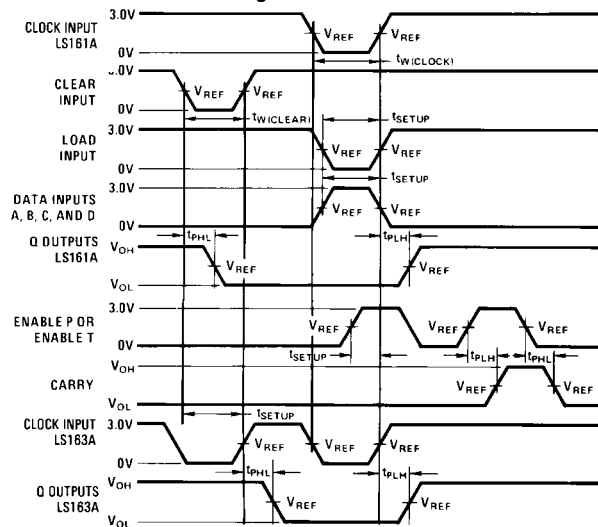
The input pulses are supplied by generators having the following characteristics:
 PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{OUT} = 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Vary PRR to measure f_{MAX} .

Outputs Q_D and carry are tested at t_{N+16} where t_N is the bit time when all outputs are LOW.

$V_{REF} = 1.5V$.

Switching Time Waveforms



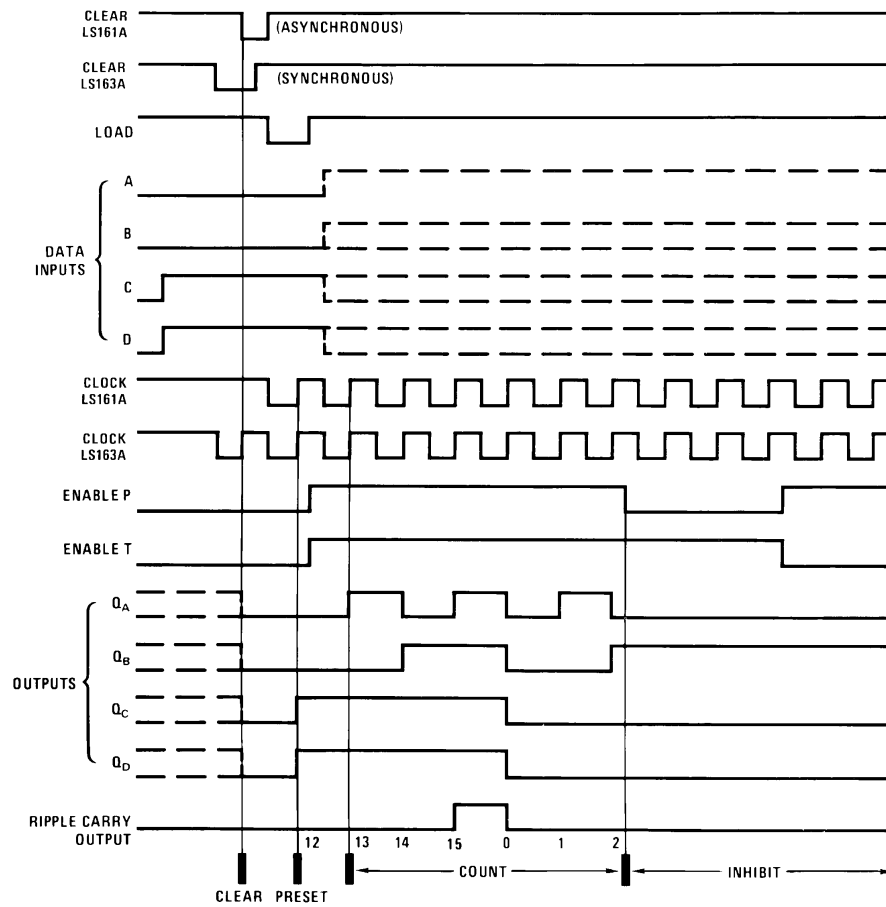
The input pulses are supplied by generators having the following characteristics:
 PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{OUT} = 50\Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX} .

Enable P and enable T setup times are measured at t_{N+0} .

$V_{REF} = 1.3V$.

Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



Sequence:

- (1) Clear outputs to zero
- (2) Preset to binary twelve
- (3) Count to thirteen, fourteen, fifteen, zero, one, and two
- (4) Inhibit

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS161A Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
I _{OL}	LOW Level Output Current			8	mA
f _{CLK}	Clock Frequency (Note 2)	0		25	MHz
	Clock Frequency (Note 3)	0		20	MHz
t _w	Pulse Width (Note 2)	Clock	20	6	ns
		Clear	20	9	
	Pulse Width (Note 3)	Clock	25		ns
		Clear	25		
t _{SU}	Setup Time (Note 2)	Data	20	8	ns
		Enable P	25	17	
		Load	25	15	
	Setup Time (Note 3)	Data	20		ns
		Enable P	30		
		Load	30		
t _H	Hold Time (Note 2)	Data	0	-3	ns
		Others	0	-3	
	Hold Time (Note 3)	Data	5		ns
		Others	5		
t _{REL}	Clear Release Time (Note 2)	20			ns
	Clear Release Time (Note 3)	25			ns
T _A	Free Air Operating Temperature	0		70	°C

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

DM74LS161A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ $I_{OL} = 4 \text{ mA}$, $V_{CC} = \text{Min}$		0.35 0.25	0.5 0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7V$			0.2 0.2 0.2 0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7V$			40 40 40 20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4V$			-0.8 -0.8 -0.8 -0.4	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 5)	-20		-100	mA
I_{CCH}	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$ (Note 6)		18	31	mA
I_{CCL}	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$ (Note 7)		19	32	mA

Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ\text{C}$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CCH} is measured with the load HIGH, then again with the load LOW, with all other inputs HIGH and all outputs OPEN.

Note 7: I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs OPEN.

DM74LS161A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$

Symbol	Parameter	From (Input) To (Output)	$R_L = 2 \text{ k}\Omega$				Units
			$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load HIGH)		22		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load HIGH)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load LOW)		24		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load LOW)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Any Q		28		45	ns

DM74LS163A Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
f_{CLK}	Clock Frequency (Note 8)	0		25	MHz
	Clock Frequency (Note 9)	0		20	MHz
t_W	Pulse Width (Note 8)	Clock	20	6	ns
		Clear	20	9	
	Pulse Width (Note 9)	Clock	25		ns
		Clear	25		
t_{SU}	Setup Time (Note 8)	Data	20	8	ns
		Enable P	25	17	
		Load	25	15	
	Setup Time (Note 9)	Data	20		ns
		Enable P	30		
		Load	30		
t_H	Hold Time (Note 8)	Data	0	-3	ns
		Others	0	-3	
	Hold Time (Note 9)	Data	5		ns
		Others	5		
t_{REL}	Clear Release Time (Note 8)	20			ns
	Clear Release Time (Note 9)	25			ns
T_A	Free Air Operating Temperature	0		70	°C

Note 8: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

Note 9: $C_L = 50$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

DM74LS163A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 10)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18$ mA			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$		0.35	0.5	V
		$I_{OL} = 4$ mA, $V_{CC} = \text{Min}$		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7\text{V}$	Enable T		0.2	mA
			Clock, Clear		0.2	
			Load		0.2	
			Others		0.1	
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7\text{V}$	Enable T		40	μA
			Load		40	
			Clock, Clear		40	
			Others		20	
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$	Enable T		-0.8	mA
			Clock, Clear		-0.8	
			Load		-0.8	
			Others		-0.4	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 11)	-20		-100	mA
I_{CCH}	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$ (Note 12)		18	31	mA
I_{CCL}	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$ (Note 13)		18	32	mA

Note 10: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

Note 11: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 12: I_{CCH} is measured with the load HIGH, then again with the load LOW, with all other inputs HIGH and all outputs OPEN.

Note 13: I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs OPEN.

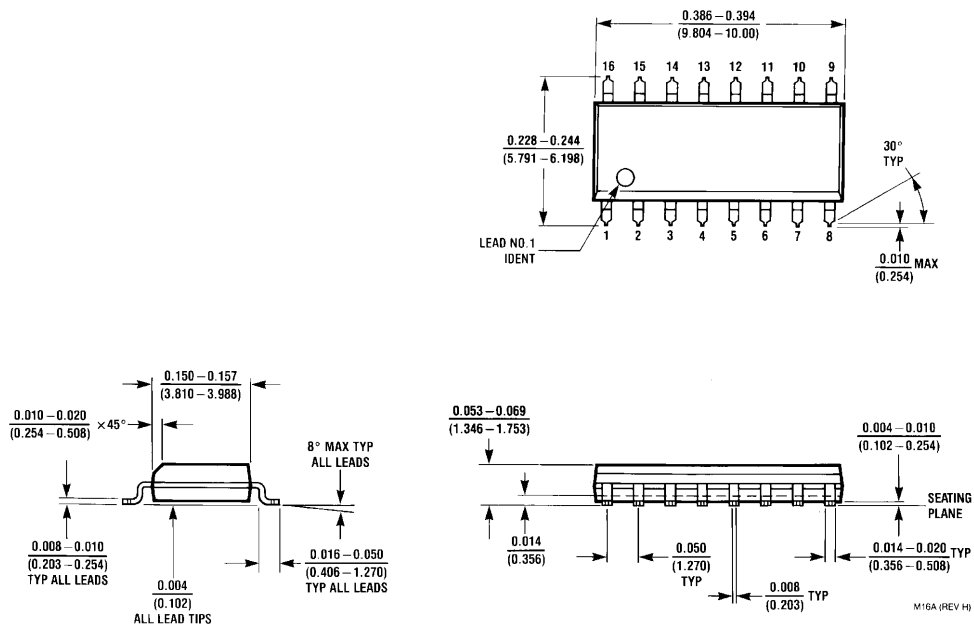
DM74LS163A Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load HIGH)		22		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load HIGH)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q (Load LOW)		24		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q (Load LOW)		27		38	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Any Q (Note 14)		28		45	ns

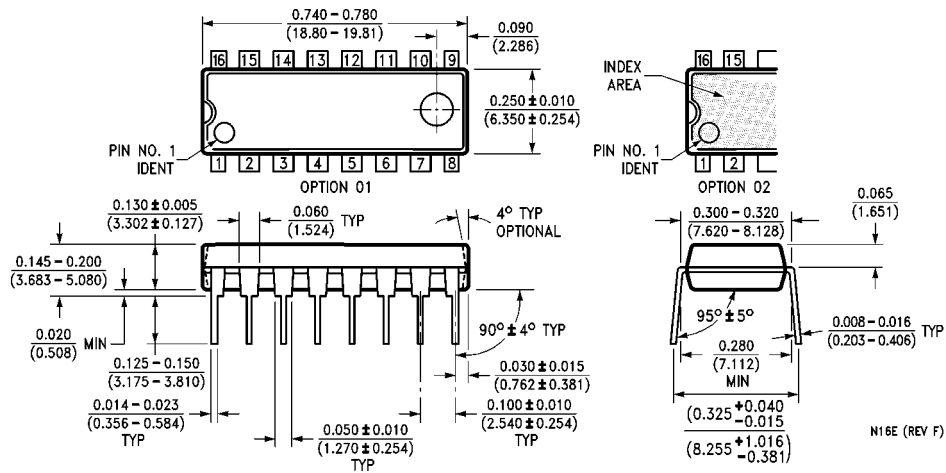
Note 14: The propagation delay clear to output is measured from the clock input transition.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Features

- Fast Read Access Time – 150 ns
- Automatic Page Write Operation
 - Internal Address and Data Latches for 64 Bytes
 - Internal Control Timer
- Fast Write Cycle Times
 - Page Write Cycle Time: 3 ms or 10 ms Maximum
 - 1 to 64-byte Page Write Operation
- Low Power Dissipation
 - 50 mA Active Current
 - 200 μ A CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
 - Endurance: 10^4 or 10^5 Cycles
 - Data Retention: 10 Years
- Single $5\text{V} \pm 10\%$ Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

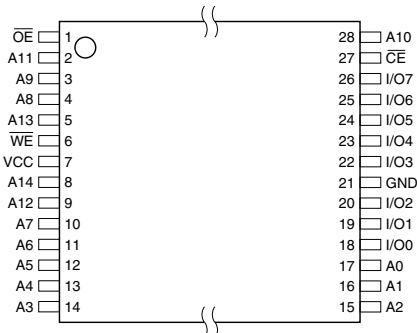
Description

The AT28C256 is a high-performance electrically erasable and programmable read only memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 200 μ A. (continued)

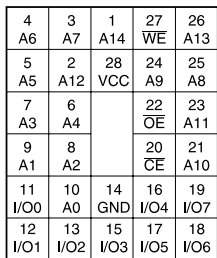
Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

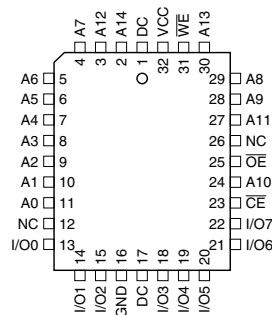
TSOP
Top View



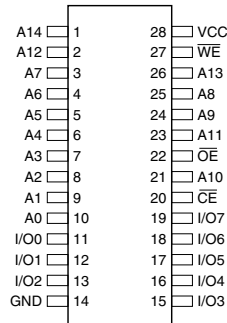
PGA
Top View



LCC, PLCC
Top View



CERDIP, PDIP, FLATPACK,
SOIC — Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.



256K (32K x 8) Paged Parallel EEPROM

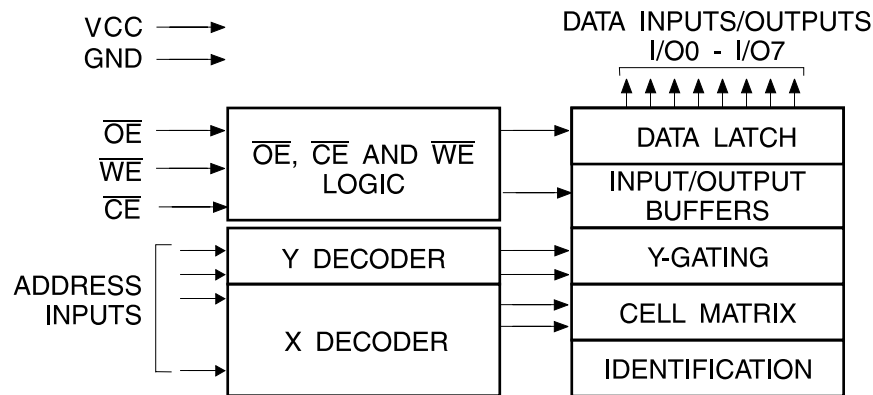
AT28C256



The AT28C256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the addresses and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of I/O₇. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's 28C256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to $V_{\text{CC}} + 0.6\text{V}$
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C256 is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 μ s (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. For each \overline{WE} high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28C256 features \overline{DATA} Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O₇. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. \overline{DATA} Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to \overline{DATA} Polling the AT28C256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O₆ toggling between one and zero. Once the write has completed, I/O₆ will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host

system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C256 in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the \overline{WE} or \overline{CE} inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to “Software Data Protection” algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28C256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28C256. This is done by preceding the data to be written by the same 3-byte command sequence used to enable SDP.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28C256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC} , read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V \pm 0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see “Software Chip Erase” application note for details.



DC and AC Operating Range

		AT28C256-15	AT28C256-20	AT28C256-25	AT28C256-35
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V _{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z
Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	High Z

- Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to AC programming waveforms.
 3. V_H = 12.0V ± 0.5V.

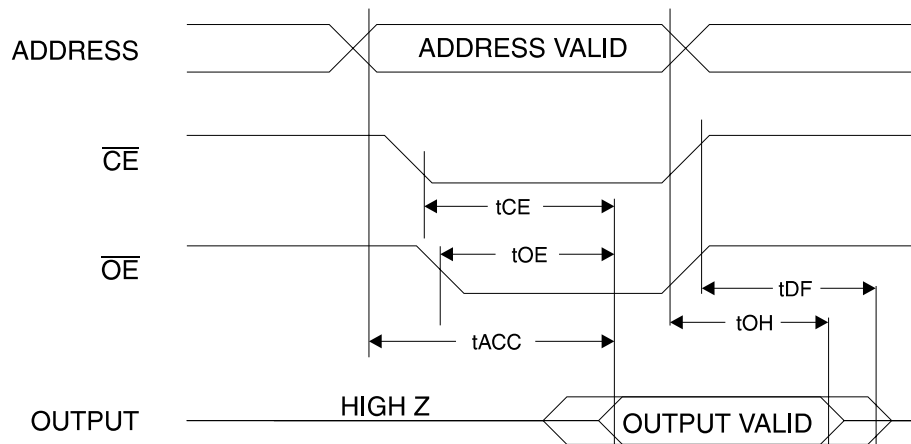
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V _{CC} + 1V	Com., Ind.	200	μA
			Mil.	300	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V _{CC} + 1V		3	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		50	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.45	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

AC Read Characteristics

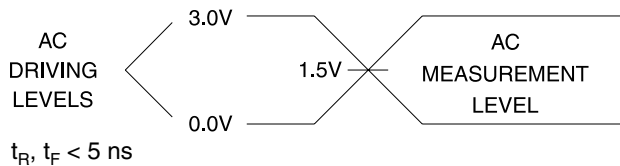
Symbol	Parameter	AT28C256-15		AT28C256-20		AT28C256-25		AT28C256-35		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250		350	ns
$t_{CE}^{(1)}$	\overline{CE} to Output Delay		150		200		250		350	ns
$t_{OE}^{(2)}$	\overline{OE} to Output Delay	0	70	0	80	0	100	0	100	ns
$t_{DF}^{(3)(4)}$	\overline{CE} or \overline{OE} to Output Float	0	50	0	55	0	60	0	70	ns
t_{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		0		0		0		ns

AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

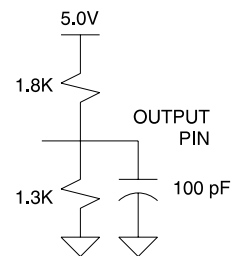


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5$ pF).
 - This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

$f = 1$ MHz, $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

- Note:
- This parameter is characterized and is not 100% tested.

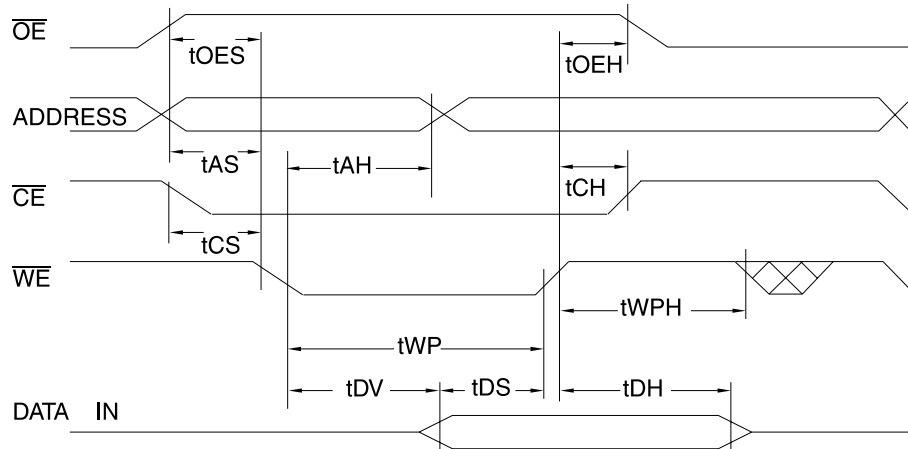
AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, \overline{OE} Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (\overline{WE} or \overline{CE})	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, \overline{OE} Hold Time	0		ns
t_{DV}	Time to Data Valid	NR ⁽¹⁾		

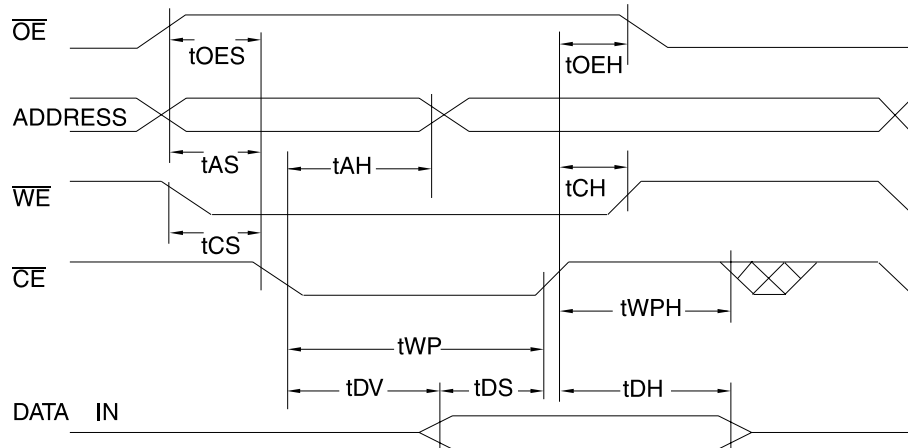
Note: 1. NR = No Restriction

AC Write Waveforms

\overline{WE} Controlled



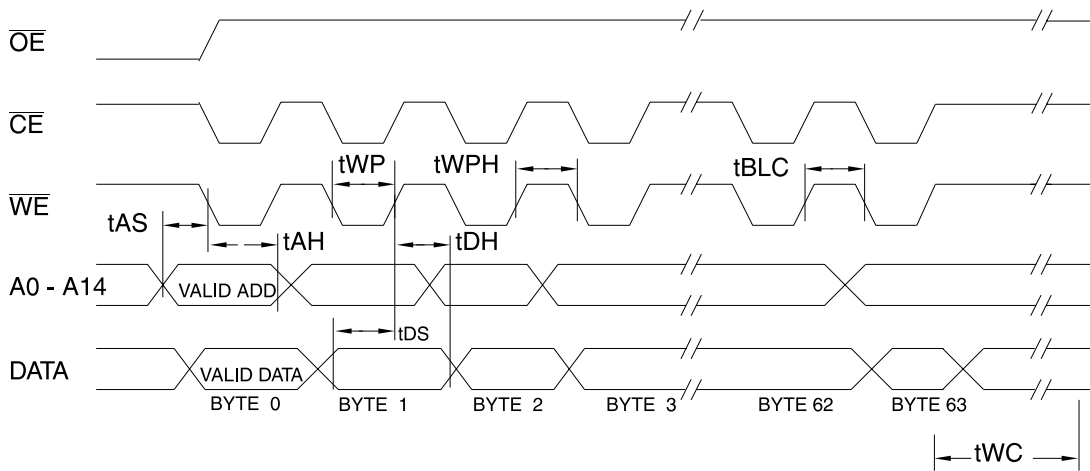
\overline{CE} Controlled



Page Mode Characteristics

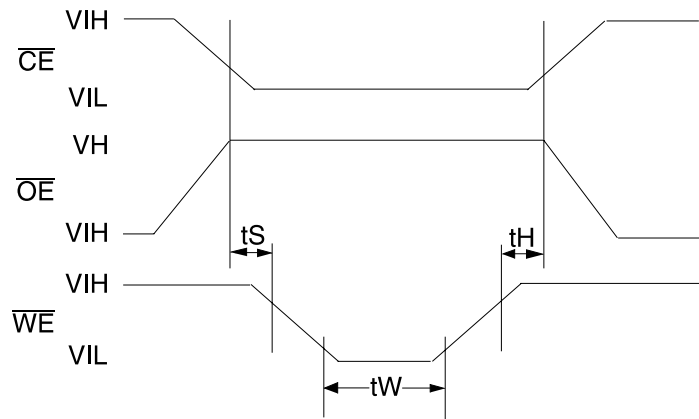
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time (option available)	AT28C256	10	ms
		AT28C256F	3	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	μ s
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms⁽¹⁾⁽²⁾



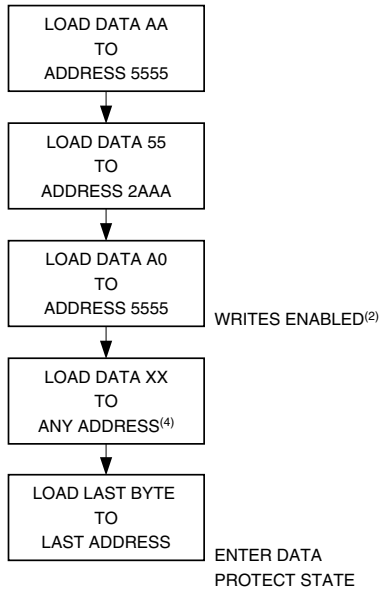
- Notes:
1. A_6 through A_{14} must specify the same page address during each high to low transition of \overline{WE} (or \overline{CE}).
 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

Chip Erase Waveforms

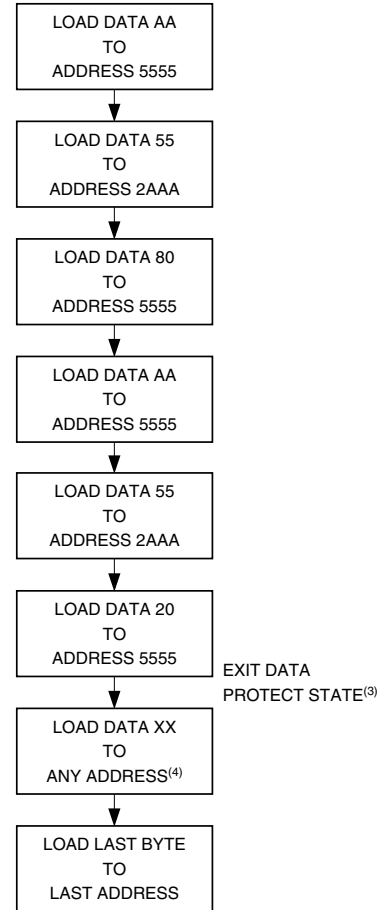


$t_S = t_H = 5 \mu\text{sec (min.)}$
 $t_W = 10 \text{ msec (min.)}$
 $V_H = 12.0V \pm 0.5V$

Software Data Protection Enable Algorithm⁽¹⁾



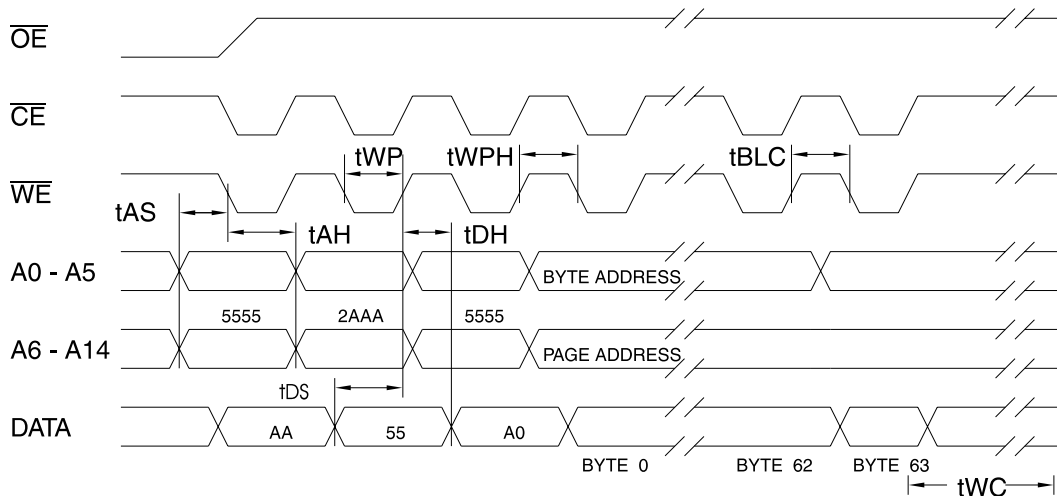
Software Data Protection Disable Algorithm⁽¹⁾



Notes for software program code:

1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms⁽¹⁾⁽²⁾



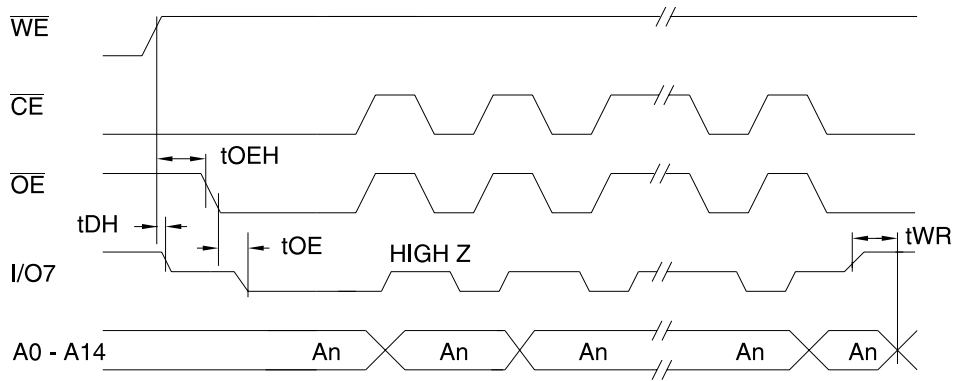
- Notes:
1. A6 through A14 must specify the same page address during each high to low transition of \overline{WE} (or \overline{CE}) after the software code has been entered.
 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
$t_{OE\overline{H}}$	\overline{OE} Hold Time	0			ns
t_{OE}	\overline{OE} to Output Delay ⁽²⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
 2. See “AC Read Characteristics”.

Data Polling Waveforms

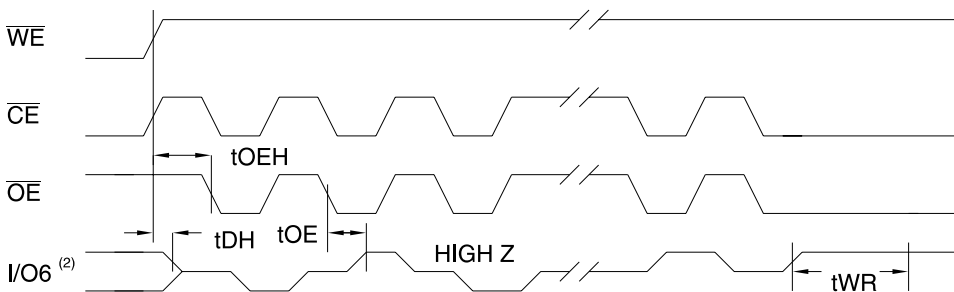


Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	\overline{OE} Hold Time	10			ns
t_{OE}	\overline{OE} to Output Delay ⁽²⁾				ns
t_{OEHP}	\overline{OE} High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

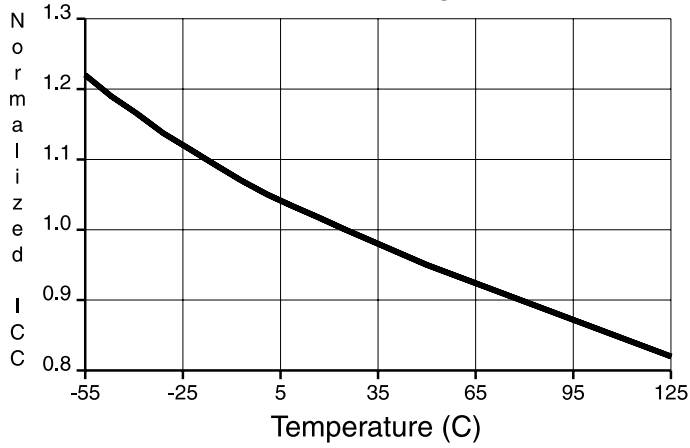
Notes: 1. These parameters are characterized and not 100% tested.
 2. See “AC Read Characteristics”.

Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾

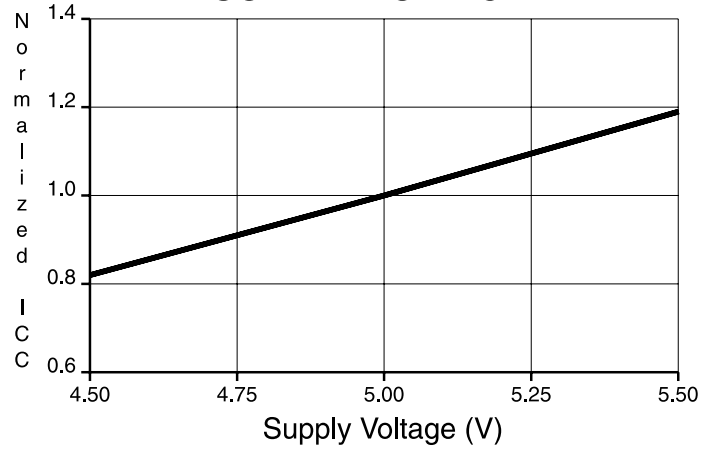


Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
 2. Beginning and ending state of I/O6 will vary.
 3. Any address location may be used but the address should not vary.

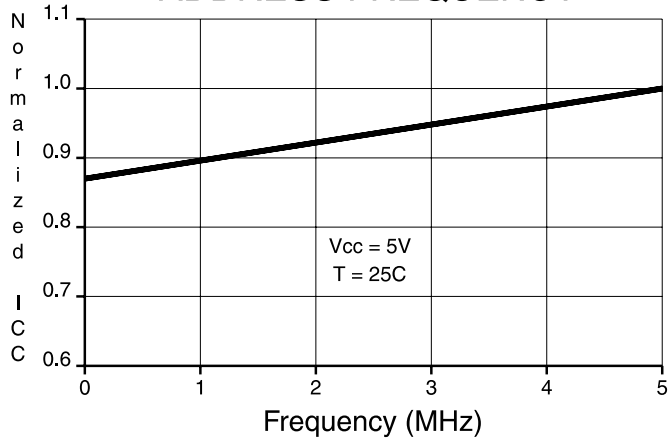
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



Ordering Information⁽²⁾

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range			
	Active	Standby						
150	50	0.2	AT28C256(E,F)-15JC	32J	Commercial (0°C to 70°C)			
			AT28C256(E,F)-15PC	28P6				
			AT28C256(E,F)-15SC	28S				
			AT28C256(E,F)-15TC	28T				
			AT28C256(E,F)-15JI	32J		Industrial (-40°C to 85°C)		
			AT28C256(E,F)-15PI	28P6				
	AT28C256(E,F)-15SI	28S						
	AT28C256(E,F)-15TI	28T						
	50	0.3	AT28C256(E,F)-15DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)			
			AT28C256(E,F)-15FM/883	28F				
			AT28C256(E,F)-15LM/883	32L				
			AT28C256(E,F)-15UM/883	28U				
200			50	0.2		AT28C256(E,F)-20JC	32J	Commercial (0°C to 70°C)
						AT28C256(E,F)-20PC	28P6	
	AT28C256(E,F)-20SC	28S						
	AT28C256(E,F)-20TC	28T						
	AT28C256(E,F)-20JI	32J			Industrial (-40°C to 85°C)			
	AT28C256(E,F)-20PI	28P6						
AT28C256(E,F)-20SI	28S							
AT28C256(E,F)-20TI	28T							
50	0.3	AT28C256(E,F)-20DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)				
		AT28C256(E,F)-20FM/883	28F					
		AT28C256(E,F)-20LM/883	32L					
		AT28C256(E,F)-20UM/883	28U					

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32L	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)
28U	28-pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms



Ordering Information⁽²⁾

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range	
	Active	Standby				
250	50	0.2	AT28C256(E,F)-25JC	32J	Commercial (0°C to 70°C)	
			AT28C256(E,F)-25PC	28P6		
			AT28C256-W	DIE		
	50	0.3	AT28C256(E,F)-25JI	32J	Industrial (-40°C to 85°C)	
			AT28C256(E,F)-25PI	28P6		
			AT28C256(E,F)-25DM/883	28D6		Military/883C Class B, Fully Compliant (-55°C to 125°C)
AT28C256(E,F)-25FM/883	28F					
AT28C256(E,F)-25LM/883	32L					
AT28C256(E,F)-25UM/883	28U					
150 ⁽³⁾	50	0.35	AT28C256(E,F)-35UM/883	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)	
			5962-88525 16 UX	28U		
			5962-88525 16 XX	28D6		
			5962-88525 16 YX	32L		
			5962-88525 16 ZX	28F		
			5962-88525 15 UX	28U		Military/883C Class B, Fully Compliant (-55°C to 125°C)
	5962-88525 15 XX	28D6				
	5962-88525 15 YX	32L				
	5962-88525 15 ZX	28F				
	50	0.35	0.35	5962-88525 14 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
				5962-88525 14 XX	28D6	
				5962-88525 14 YX	32L	
5962-88525 14 ZX				28F		

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32L	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28U	28-pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Ordering Information⁽²⁾

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range	
	Active	Standby				
150 ⁽³⁾	50	0.35	5962-88525 08 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)	
			5962-88525 08 XX	28D6		
			5962-88525 08 YX	32L		
			5962-88525 08 ZX	28F		
				5962-88525 07 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
				5962-88525 07 XX	28D6	
				5962-88525 07 YX	32L	
				5962-88525 07 ZX	28F	
				5962-88525 06 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
				5962-88525 06 XX	28D6	
				5962-88525 06 YX	32L	
				5962-88525 06 ZX	28F	
200 ⁽³⁾	50	0.35	5962-88525 12 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)	
			5962-88525 12 XX	28D6		
			5962-88525 12 YX	32L		
			5962-88525 12 ZX	28F		
	50	0.35	5962-88525 04 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)	
			5962-88525 04 XX	28D6		
			5962-88525 04 YX	32L		
			5962-88525 04 ZX	28F		
250 ⁽³⁾	50	0.35	5962-88525 13 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)	
			5962-88525 13 XX	28D6		
			5962-88525 13 YX	32L		
			5962-88525 13 ZX	28F		
				5962-88525 11 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
				5962-88525 11 XX	28D6	
				5962-88525 11 YX	32L	
				5962-88525 11 ZX	28F	

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32L	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28U	28-pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms





Ordering Information⁽²⁾

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	50	0.35	5962-88525 05 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 05 XX	28D6	
			5962-88525 05 YX	32L	
			5962-88525 05 ZX	28F	
	5962-88525 03 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)		
				5962-88525 03 XX	28D6
				5962-88525 03 YX	32L
				5962-88525 03 ZX	28F
300	50	0.35	5962-88525 10 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 10 XX	28D6	
			5962-88525 10 YX	32L	
			5962-88525 10 ZX	28F	
	5962-88525 02 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)		
				5962-88525 02 XX	28D6
				5962-88525 02 YX	32L
				5962-88525 02 ZX	28F
350	50	0.35	5962-88525 09 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			5962-88525 09 XX	28D6	
			5962-88525 09 YX	32L	
			5962-88525 09 ZX	28F	
	5962-88525 01 UX	28U	Military/883C Class B, Fully Compliant (-55°C to 125°C)		
				5962-88525 01 XX	28D6
				5962-88525 01 YX	32L
				5962-88525 01 ZX	28F

- Notes:
1. Electrical specifications for these speeds are defined by Standard Microcircuit Drawing 5962-88525.
 2. See "Valid Part Numbers" table below.
 3. SMD specifies Software Data Protection feature for device type, although Atmel product supplied to every device type in the SMD is 100% tested for this feature.

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32L	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28U	28-pin, Ceramic Pin Grid Array (PGA)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

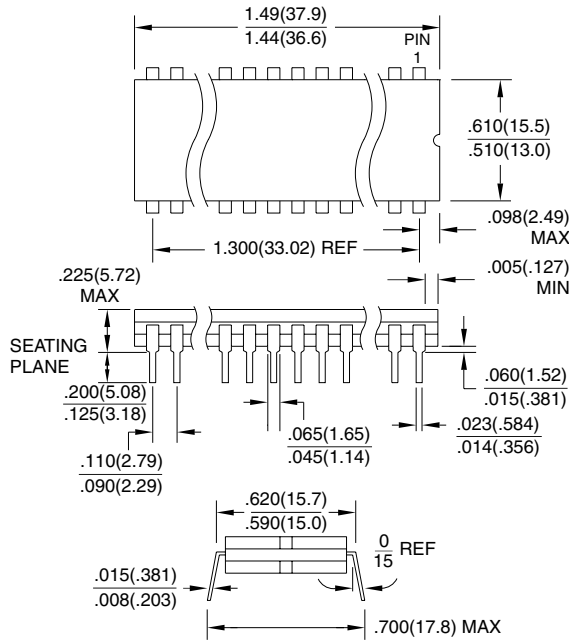
Device Numbers	Speed	Package and Temperature Combinations
AT28C256	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	15	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	20	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256E	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256F	25	JC, JI, PC, PI, SC, SI, TC, TI, DM/883, FM/883, LM/883, UM/883
AT28C256	–	W

Die Products

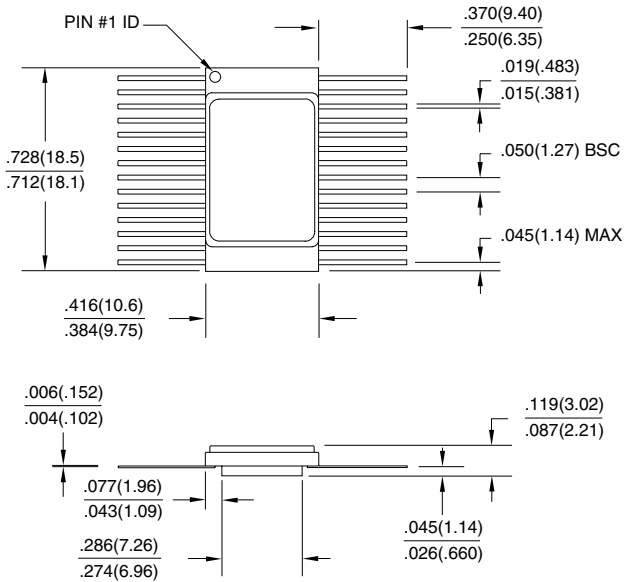
Reference Section: Parallel EEPROM Die Products

Packaging Information

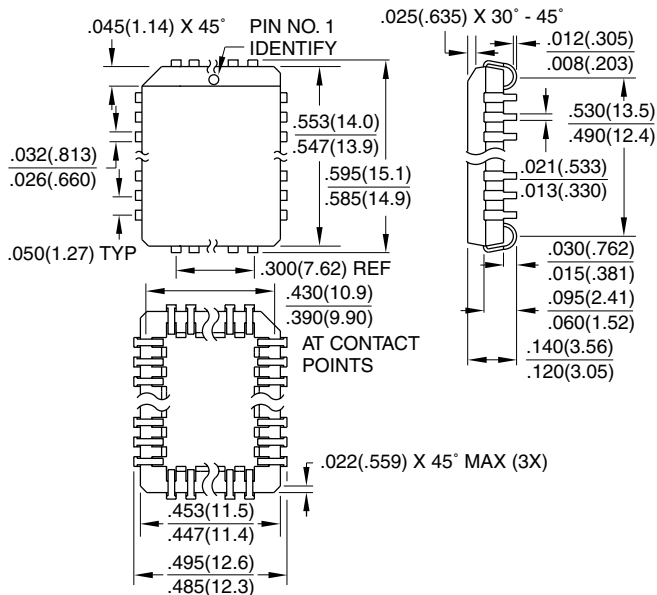
28D6, 28-lead, 0.600" Wide, Non-windowed Ceramic Dual Inline Package (Cerdip)
 Dimensions in Inches and (Millimeters)
 MIL-STD-1835 D-10 CONFIG A



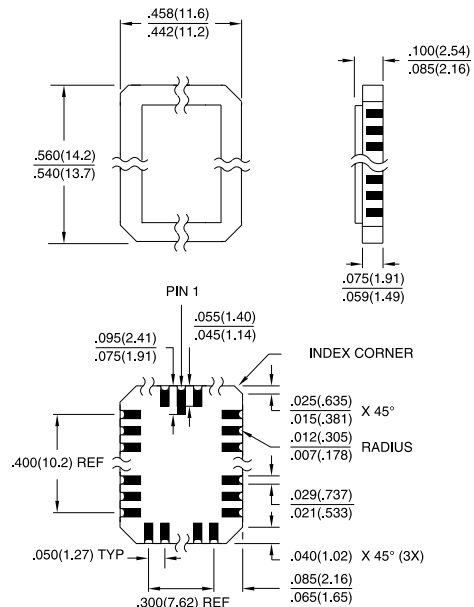
28F, 28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
 Dimensions in Inches and (Millimeters)
 MIL-STD-1835 F-12 CONFIG B



32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)
 Dimensions in Inches and (Millimeters)
 JEDEC STANDARD MS-016 AE



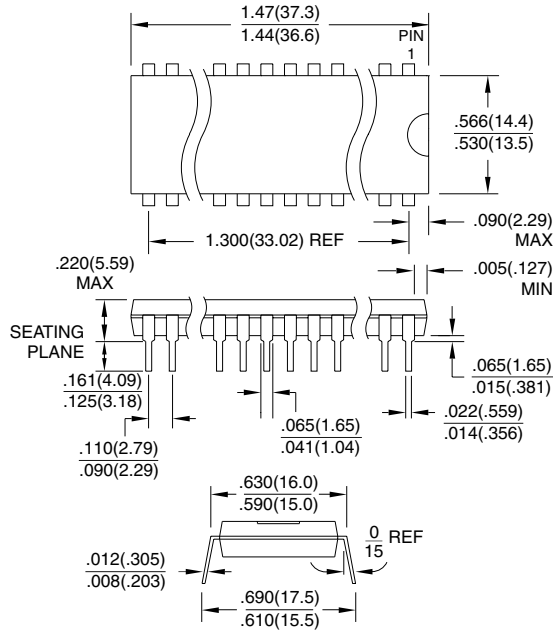
32L, 32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
 Dimensions in Inches and (Millimeters)
 MIL-STD-1835 C-12



Packaging Information

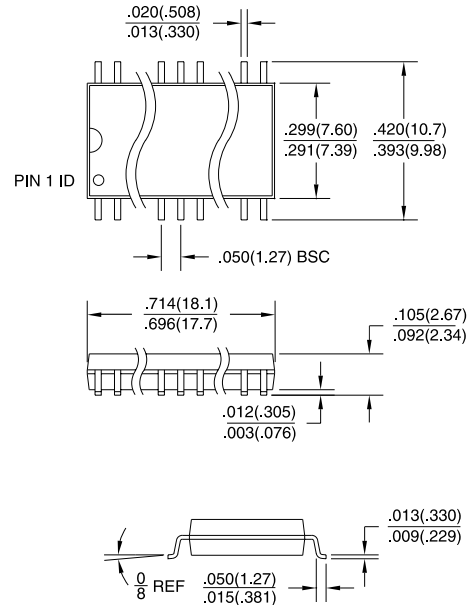
28P6, 28-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)

Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AB



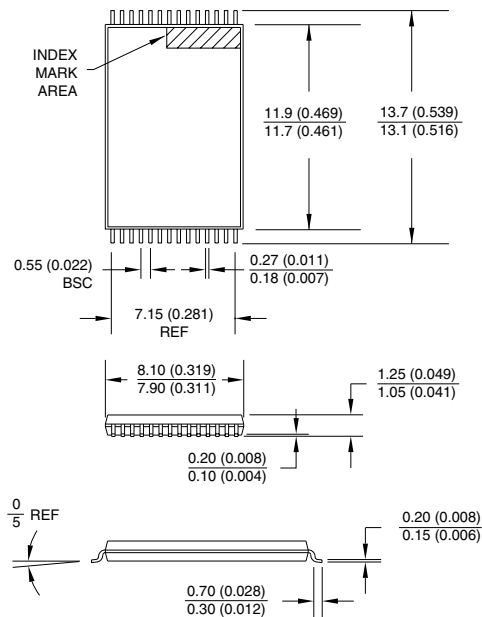
28S, 28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)

Dimensions in Inches and (Millimeters)



28T, 28-lead, Plastic Thin Small Outline Package (TSOP)

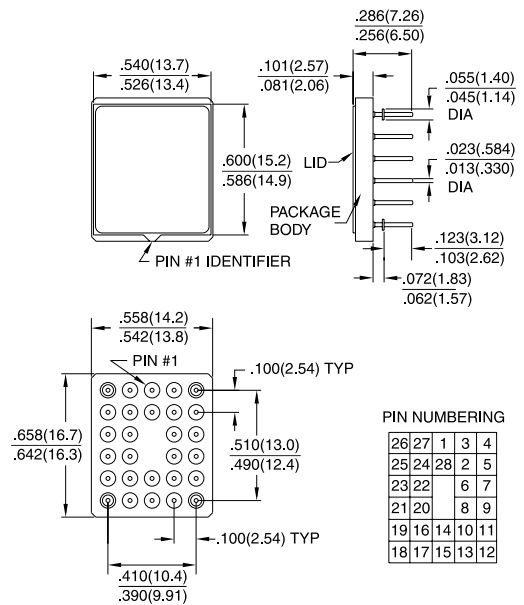
Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters

28U, 28-pin, Ceramic Pin Grid Array (PGA)

Dimensions in Inches and (Millimeters)





Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan

Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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