LTC1266
LTC1266-3.3/LTC1266-5

Synchronous Regulator Controller for N- or P-Channel MOSFETs

FEATURES

- **Ultrahigh Efficiency: Over 95% Possible**
- **Drives N-Channel MOSFET for High Current or P-Channel MOSFET for Low Dropout**
- Pin Selectable Burst Mode Operation
- 1% Output Accuracy (LTC1266A)
- Pin Selectable Phase of Topside Driver for Boost or Step-Down Operation
- Wide V_{IN} Range: 3.5V to 20V
- On-Chip Low-Battery Detector
- High Efficiency Maintained Over Large Current Range
- Low 170µA Standby Current at Light Loads
- Current Mode Operation for Excellent Line and Load Transient Response
- Logic Controlled Micropower Shutdown: I_Q < 40µA
- Short-Circuit Protection
- Synchronous Switching with Nonoverlaping Gate Drives
- Available in 16-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Cellular Telephones
- DC Power Distribution Systems
- GPS Systems

DESCRIPTION

The LTC®1266 series is a family of synchronous switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external power MOSFETs at switching frequencies up to 400kHz using a constant off-time current mode architecture providing constant ripple current in the inductor. They can drive either an N-channel or a P-channel topside MOSFET.

The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 18V (20V maximum). Constant off-time architecture provides low dropout regulation limited only by the $R_{DS(ON)}$ of the topside MOSFET (when using the P-channel) and the resistance of the inductor and current sense resistor.

The LTC1266 series combines synchronous switching for maximum efficiency at high currents with an automatic low current operating mode, called Burst Mode operation, which reduces switching losses. Standby power is reduced to only 1mW at V_{IN} = 5V (at I_{OUT} = 0). Load currents in Burst Mode operation are typically 0mA to 500mA.

TYPICAL APPLICATION

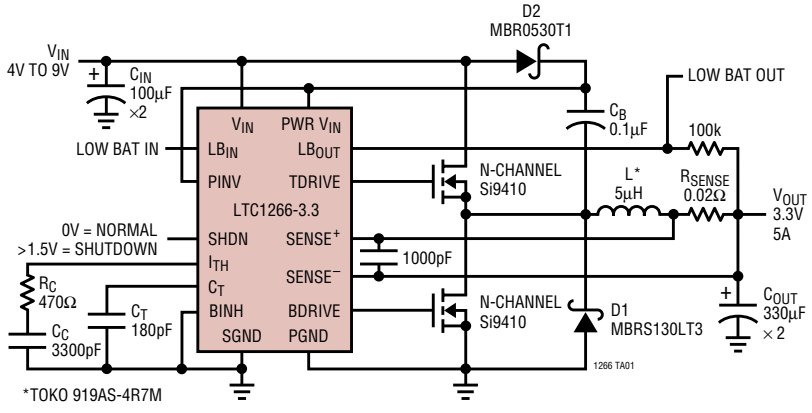
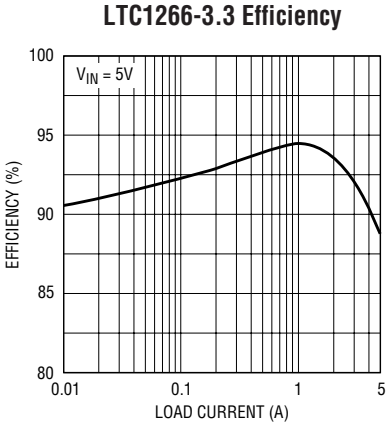


Figure 1. High Efficiency Step-Down Converter

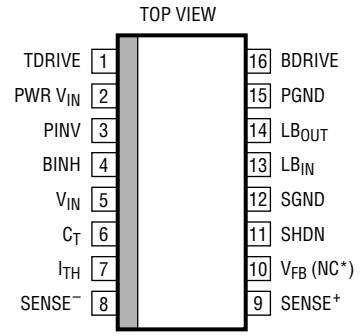


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (Pins 2, 5) ..... 20V to –0.3V
Continuous Output Current (Pins 1, 16) 50mA
Sense Voltages (Pins 8, 9) ..... 13V to –0.3V
SHDN Voltage (Pin 11) ..... 12V to –0.3V
PINV, BINH, LB_{IN} (Pins 3, 4, 13) ..... 20V to –0.3V
LB_{OUT} Output Current 12mA
Operating Ambient Temperature Range ..... 0°C to 70°C
Industrial Temperature Range ..... –40°C to 85°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1266CS
LTC1266CS-3.3
LTC1266CS-5
LTC1266ACS
LTC1266IS
LTC1266IS-3.3
LTC1266IS-5
LTC1266AIS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, V_{SHDN} = V_{BINH} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage	V_{IN} = 9V, I_{LOAD} = 700mA, V_{PINV} = V_{PWR} = 14V, Topside Switch = N-Ch					
	LTC1266ACS		●	1.252	1.265	1.278	V
	LTC1266CS		●	1.210	1.265	1.290	V
I_{FB}	Feedback Current (LTC1266 Only)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V, I_{LOAD} = 700mA, V_{PINV} = V_{PWR} = 14V, Topside Switch = N-Ch					
	LTC1266CS-3.3		●	3.23	3.33	3.43	V
	LTC1266CS-5		●	4.90	5.05	5.20	V
	Output Ripple (Burst Mode Operation)	I_{LOAD} = 150mA			50		mV_{P-P}
ΔV_{OUT}	Output Voltage Line Regulation	I_{LOAD} = 50mA					
		V_{PINV} = 0V, Topside Switch = P-Ch, V_{IN} = 7V to 12V		–40	0	40	mV
		V_{PINV} = V_{PWR}, Topside Switch = N-Ch, V_{IN} = 7V to 12V		–40	0	40	mV
	Output Voltage Load Regulation	5mA < I_{LOAD} < 2A, R_{SENSE} = 0.05Ω					
	LTC1266-3.3	Burst Mode Operation Enabled, V_{BINH} = 0V	●		40	65	mV
	LTC1266-3.3	Burst Mode Operation Inhibited, V_{BINH} = 2V	●		15	25	mV
	LTC1266-5	Burst Mode Operation Enabled, V_{BINH} = 0V	●		60	100	mV
	LTC1266-5	Burst Mode Operation Inhibited, V_{BINH} = 2V	●		25	40	mV
I_{Q1}	V_{IN} Pin DC Supply Current (Note 3)						
	Normal Mode	3.5V < V_{IN} < 18V			2.1	3.0	mA
	Sleep Mode	3.5V < V_{IN} < 18V			170	250	µA
	Shutdown	V_{SHDN} = 2.1V, 3.5V < V_{IN} < 18V			25	50	µA
I_{Q2}	PWR V_{IN} DC Supply Current (Note 3)						
	Normal Mode	3.5V < PWR V_{IN} < 18V			20	40	µA
	Sleep Mode	3.5V < PWR V_{IN} < 18V			1	5	µA
	Shutdown	V_{SHDN} = 2.1V, 3.5V < PWR V_{IN} < 18V			1	5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, V_{SHDN} = V_{BINH} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SENSE\ 1}$	Current Sense Threshold (Burst Mode Operation Enabled)	V_{BINH} = 0V					
	LTC1266	V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	●	135	155	175	mV
	LTC1266-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	135	155	175	mV
	LTC1266-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	135	155	175	mV
$V_{SENSE\ 2}$	Current Sense Threshold (Burst Mode Operation Disabled)	V_{BINH} = 2.1V					
	LTC1266	V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 + 25mV (Forced)			–20		mV
		V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	●	135	155	175	mV
	LTC1266-3.3	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			–20		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	135	155	175	mV
	LTC1266-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)			–20		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	135	155	175	mV
V_{SHDN}	Shutdown Pin Threshold			0.6	0.8	2	V
I_{SHDN}	Shutdown Pin Input Current	0V < V_{SHDN} < 8V, V_{IN} = 16V			1.2	5	µA
I_{PINV}	Phase Invert Pin Input Current	0V < V_{PINV} < 18V, V_{IN} = 18V			0.2	1	µA
V_{BINH}	Burst Mode Operation Inhibit Pin Threshold	V_{IN} = 7V		0.8	1.2	2	V
I_{BINH}	Burst Mode Operation Inhibit Pin Input Current	0V < V_{BINH} < 18V, V_{IN} = 18V			0.2	1	µA
I_{CT}	C_T Pin Discharge Current	V_{SENSE}^+ = V_{OUT} – 100mV, V_{SENSE}^- = V_{OUT} – 300mV		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µs
t_{MAX}	Max On-Time	V_{OUT} = 0V, V_{IN} = 18V			60		µs
t_r, t_f	Driver Output Transition Times (Note 7)	C_L = 3000pF (Pins 1, 16), V_{IN} = 6V			100	200	ns
V_{CLAMP}	Output Voltage Clamp in Burst Mode Operation Inhibit	V_{BINH} = 2.1V					
	LTC1266	Measured at V_{FB}			1.30		V
	LTC1266-3.3	Measured at V_{SENSE}^-			3.43		V
	LTC1266-5	Measured at V_{SENSE}^-			5.20		V
V_{LBTRIP}	Low-Battery Trip Point	V_{IN} = 5V		1.14	1.25	1.35	V
		V_{IN} = 12V		1.17	1.30	1.42	V
I_{LBLEAK}	Max Leakage Current Into Pin 14	V_{LBOUT} = 18V, V_{LBIN} = 2V			25	200	nA
I_{LBSINK}	Max Sink Current Into Pin 14	V_{LBOUT} = 1V, V_{LBIN} = 0V, 2.5V < V_{IN} < 18V		1	8		mA
I_{LBIN}	Max Leakage Current Into Pin 13	V_{LBIN} = 18V			0.2	1	µA

–40°C < T_A < 85°C (Note 5), V_{IN} = 10V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage	V_{IN} = 9V, I_{LOAD} = 700mA, V_{PINV} = V_{PWR} = 14V, Topside Switch = N-Ch				
	LTC1266AIS		1.246	1.265	1.290	V
	LTC1266CS, LTC1266IS		1.210	1.265	1.290	V
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V, I_{LOAD} = 700mA, V_{PINV} = V_{PWR} = 14, Topside Switch = N-Ch				
	LTC1266CS-3.3, LTC1266IS-3.3		3.23	3.33	3.43	V
	LTC1266CS-5, LTC1266IS-5		4.90	5.05	5.20	V

ELECTRICAL CHARACTERISTICS

–40°C < T_A < 85°C (Note 5), V_{IN} = 10V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{Q1}	V_{IN} Pin DC Supply Current (Note 3)					
	Normal Mode	3.5V < V_{IN} < 18V		2.1	3.3	mA
	Sleep Mode	3.5V < V_{IN} < 18V		170	260	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 3.5V < V_{IN} < 18V		25	60	µA
I_{Q2}	PWR V_{IN} DC Supply Current (Note 3)					
	Normal Mode	3.5V < PWR V_{IN} < 18V		20	50	µA
	Sleep Mode	3.5V < PWR V_{IN} < 18V		1	7	µA
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 3.5V < PWR V_{IN} < 18V		1	7	µA
V_{SENSE1}	Current Sense Threshold (Burst Mode Operation Enabled)	V_{BINH} = 0V				
	LTC1266CS, LTC1266IS	V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 + 25mV (Forced)		25		mV
	LTC1266CS	V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	135	155	180	mV
	LTC1266IS	V_{SENSE}^- = 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	135	155	190	mV
	LTC1266-3.3, LTC1266-5 (I and C)	V_{SENSE}^- = V_{OUT} + 100mV (Forced)		25		mV
	LTC1266CS-3.3, LTC1266CS-5	V_{SENSE}^- = V_{OUT} – 100mV (Forced)	135	155	180	mV
	LTC1266IS-3.3, LTC1266IS-5	V_{SENSE}^- = V_{OUT} – 100mV (Forced)	135	155	190	mV
V_{SENSE2}	Current Sense Threshold (Burst Mode Operation Disabled)	V_{BINH} = 2.1V				
	LTC1266CS, LTC1266IS	V_{SENSE}^- 3.3V, V_{FB} = V_{OUT}/2.64 + 25mV (Forced)		–20		mV
	LTC1266CS	V_{SENSE}^- 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	130	155	185	mV
	LTC1266IS	V_{SENSE}^- 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	130	155	195	mV
	LTC1266-3.3, LTC1266-5 (I and C)	V_{SENSE}^- = V_{OUT} + 100mV (Forced)		–20		mV
	LTC1266CS-3.3, LTC1266CS-5	V_{SENSE}^- = V_{OUT} – 100mV (Forced)	130	155	185	mV
	LTC1266IS-3.3, LTC1266IS-5	V_{SENSE}^- = V_{OUT} – 100mV (Forced)	130	155	195	mV
V_{SHDN}	Shutdown Pin Threshold	C Grade	0.55	0.8	2	V
		I Grade	0.50	0.8	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, C Grade	3.8	5	6.5	µs
		C_T = 390pF, I_{LOAD} = 700mA, I Grade	3.8	5	7.0	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \times 110°C/W)$

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

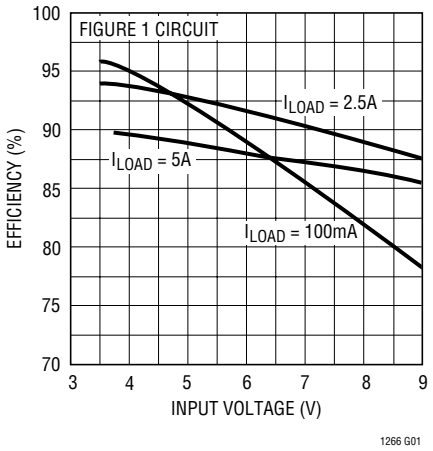
Note 5: The LTC1266CS, LTC1266CS-3.3, LTC1266-5 and LTC1266ACS are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation. The LTC1266IS, LTC1266IS-3.3, LTC1266IS-5 and LTC1266AIS are guaranteed and tested over the –40°C to 85°C operating temperature range.

Note 6: Unless otherwise noted the specifications for the LTC1266A are the same as those for the LTC1266.

Note 7: t_r and t_f are measured at 10% and 90% levels.

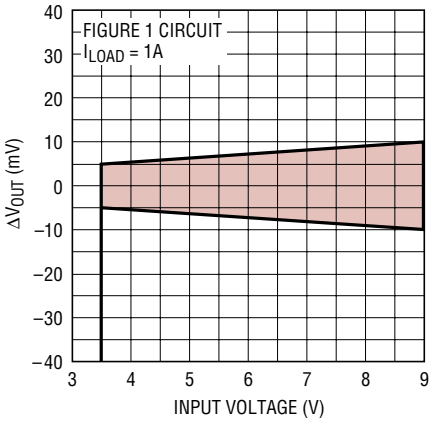
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



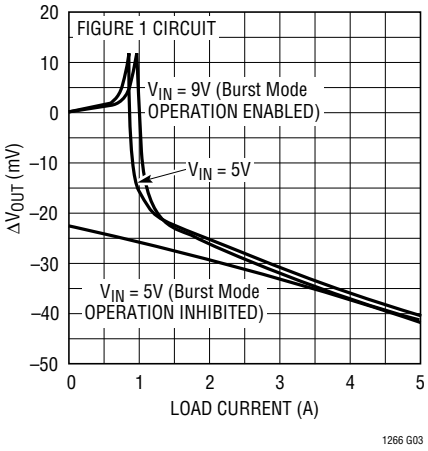
1266 G01

Line Regulation



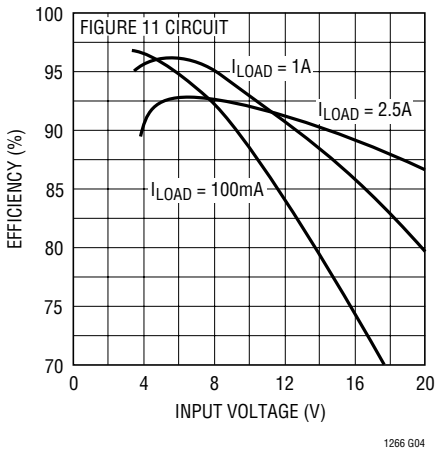
1266 G02

Load Regulation



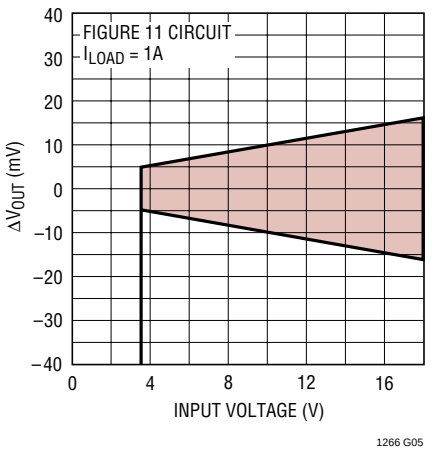
1266 G03

Efficiency vs Input Voltage



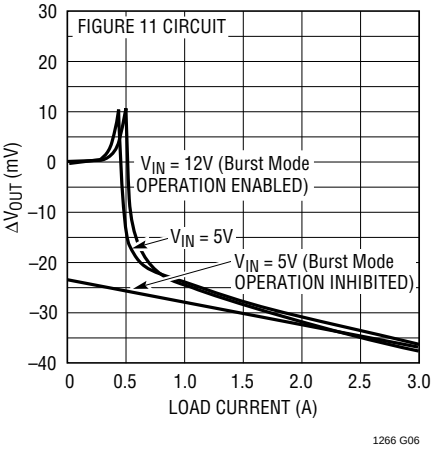
1266 G04

Line Regulation



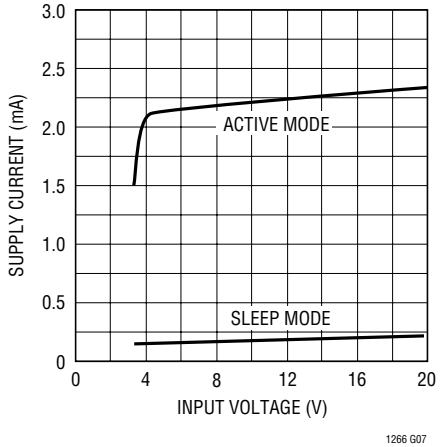
1266 G05

Load Regulation



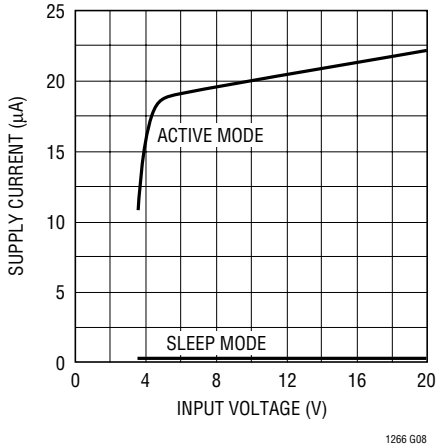
1266 G06

V_{IN} DC Supply Current



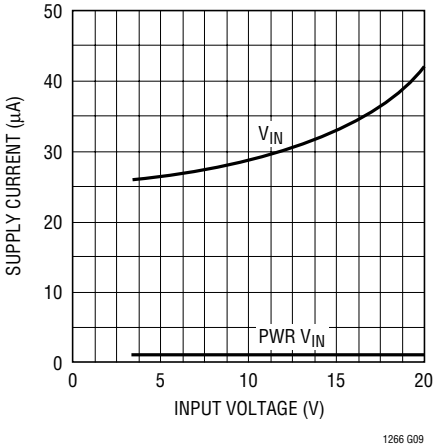
1266 G07

Power V_{IN} DC Supply Current



1266 G08

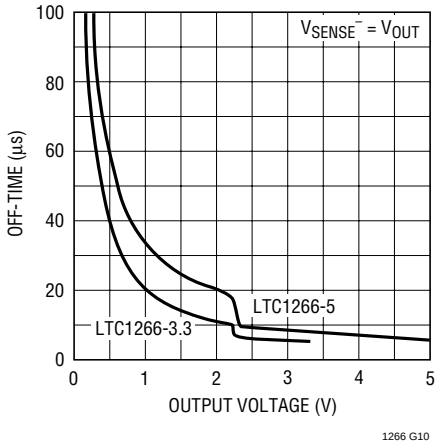
Supply Current in Shutdown



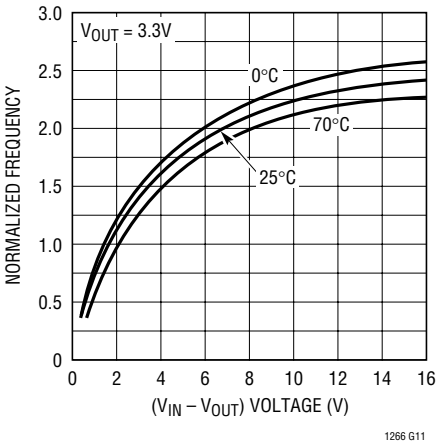
1266 G09

TYPICAL PERFORMANCE CHARACTERISTICS

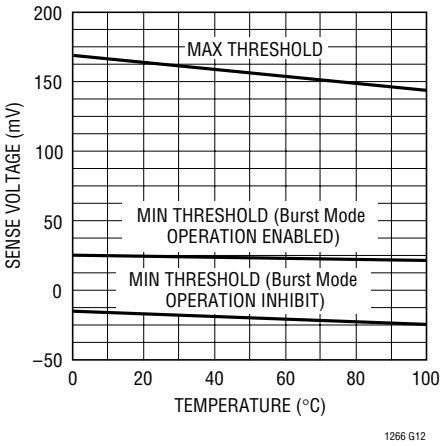
Off-Time vs Output Voltage



Operating Frequency vs (V_{IN} – V_{OUT}) Voltage



Current Sense Threshold Voltage



PIN FUNCTIONS

TDRIVE (Pin 1): High Current Drive for Topside MOSFET. This MOSFET can be either P-channel or N-channel, user selectable by Pin 3. Voltage swing at this pin is from PWR V_{IN} to ground.

PWR V_{IN} (Pin 2): Power Suppy for Drive Signals. Must be closely decoupled to power ground (Pin 15).

PINV (Pin 3): Phase Invert. Sets the phase of the topside driver to drive either a P-channel or an N-channel MOSFET as follows:

P-channel: Pin 3 = 0V
N-channel: Pin 3 = PWR V_{IN}

BINH (Pin 4): Burst Mode Operation Inhibit. A CMOS logic high on this pin will disable the Burst Mode operation feature forcing continuous operation down to zero load.

V_{IN} (Pin 5): Main Supply Pin.

C_T (Pin 6): External Capacitor. C_T from Pin 4 to ground sets the operating frequency. The actual frequency is also dependent on the input voltage.

I_{TH} (Pin 7): Gain Amplifier Decoupling Point. The current comparator threshold increases with the Pin 7 voltage.

SENSE$^-$ (Pin 8): Connects to internal resistive divider which sets the output voltage in LTC1266-3.3 and LTC1266-5 versions. Pin 8 is also the (–) input for the current comparator.

SENSE$^+$ (Pin 9): The (+) Input to the Current Comparator. A built-in offset between Pins 8 and 9 in conjunction with R_{SENSE} sets the current trip threshold.

V_{FB} (Pin 10): For the LTC1266 adjustable version, Pin 10 serves as the feedback pin from an external resistive divider used to set the output voltage. On LTC1266-3.3 and LTC1266-5 versions this pin is not used.

SHDN (Pin 11): When grounded, the LTC1266 series operates normally. Pulling Pin 11 high holds both MOSFETs off and puts the LTC1266 in micropower shutdown mode. Requires CMOS logic signal with t_r, t_f < 1µs. Should not be left floating.

SGND (Pin 12): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

LB_{IN} (Pin 13): Input to the Low-Battery Comparator. This input is compared to an internal 1.25V reference.

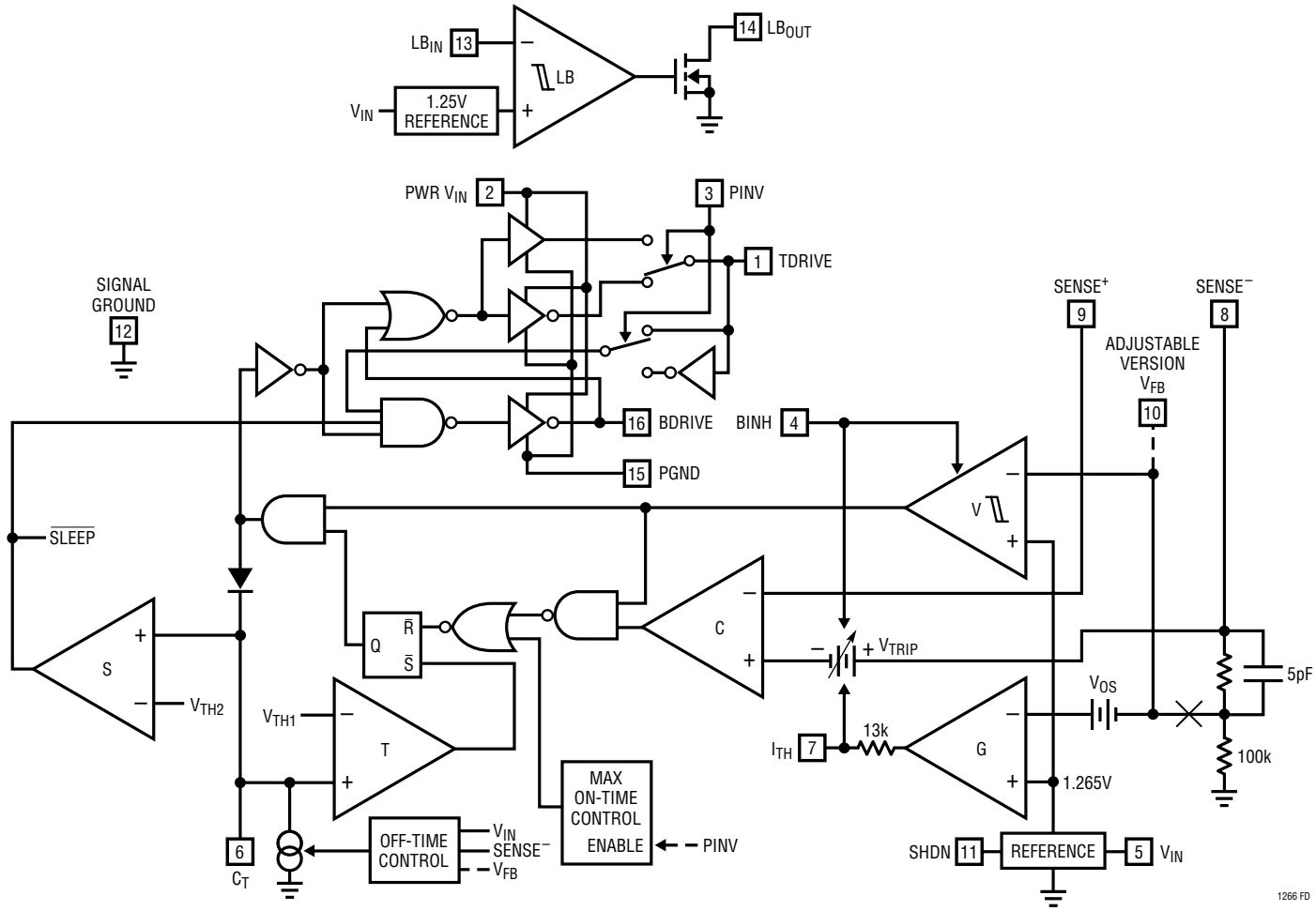
LB_{OUT} (Pin 14): Open Drain Output of the Low-Battery Comparator. This pin will sink current when Pin 13 is below 1.25V.

PGND (Pin 15): Driver Power Ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

BDRIVE (Pin 16): High Current Drive for Bottom N-Channel MOSFET. Voltage swing at Pin 16 is from ground to PWR V_{IN}.

FUNCTIONAL DIAGRAM

Pin 10 Connection Shown for LTC1266-3.3 and LTC1266-5; Changes Create LTC1266



OPERATION

The LTC1266 series uses a current mode, constant off-time architecture to synchronously switch an external pair of power MOSFETs. Operating frequency is set by an external capacitor at the timing capacitor Pin 6.

The output voltage is sensed by an internal voltage divider connected to SENSE$^-$, Pin 8, (LTC1266-3.3 and LTC1266-5) or external divider returned to V_{FB}, Pin 10, (LTC1266). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.265V. To optimize efficiency, the LTC1266 automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch ON cycle in continuous mode, current comparator C monitors the voltage between Pins 8 and 9 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the topside driver output is switched to turn off the topside MOFSET (Power V_{IN} for P-channel or ground for N-channel). The timing capacitor connected to Pin 6 is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by Pin 8) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the bottom-side drive output is switched to power V_{IN} to turn on the bottom-side N-channel MOSFET.

OPERATION

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the bottom-side output to switch off and the topside output to switch on (ground for P-channel and Power V_{IN} for N-channel). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (Pin 7) to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the topside MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep line to go low and the bottom-side MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, a majority of the circuitry is turned off, dropping the quiescent current from 2.1mA to 170μA. The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the topside MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the bottom-side drive output can turn on, the topside output must be off. Likewise, the topside output is prevented from turning on while the bottom-side drive output is still on.

The LTC1266 has two select pins which provide the user with choice of topside switch and with the option of inhibiting Burst Mode operation. The phase select pin allows the user to choose whether the topside MOSFET is a P-channel or an N-channel. The phase select pin does two things: sets the proper phase of the drive signal (ON = Power V_{IN} for N-channel and ON = 0V for P-channel) and also sets an upper limit for the on-time (60μs) when set to the N-channel. The on-time limit ensures proper start-up when used in a single supply bootstrap circuit configuration (see Applications Information). In P-channel mode there is no on-time limit and thus, in dropout, the P-channel MOSFET is turned on continuously (100% duty cycle).

The Burst Mode operation inhibit (BINH, Pin 4) allows the Burst Mode operation to be disabled by applying a CMOS logic high to this pin. With Burst Mode operation disabled, the LTC1266 will remain in continuous mode down to zero load. Burst Mode operation is disabled by allowing the lower current threshold limit to go below zero so that the voltage comparator will never trip. The voltage comparator trip point is also raised up so that it will not be tripped by transients. It is still active to provide a voltage clamp to prevent the output from overshooting.

APPLICATIONS INFORMATION

One of the three basic LTC1266 application circuits is shown in Figure 1. This circuit uses an N-channel topside driver and a single supply. The other two circuit configurations (see Typical Applications) use an N-channel topside driver and dual supply, and a P-channel topside driver. Selections of other external components are driven by the load requirement and are the same for all three circuit configurations. The first step is the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Using an N-channel topside switch, input voltages are limited to a maximum of about 15V. With a P-channel, the input voltage may be as high as 20V.

APPLICATIONS INFORMATION

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1266 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} (when Burst Mode operation is enabled) to a maximum of 155mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1266 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} vs maximum output current is given in Figure 2.

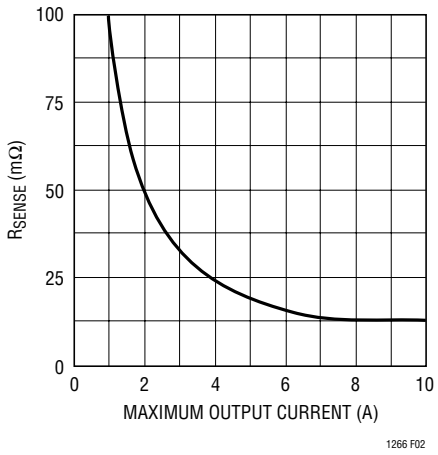


Figure 2. Selecting R_{SENSE}

The load current, below which Burst Mode operation commences, (I_{BURST}), and the peak short-circuit current, ($I_{SC(PK)}$), both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{155mV}{R_{SENSE}}$$

The LTC1266 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1266 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the topside MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{1}{2.6 \bullet 10^4 \bullet f}$$

assumes $V_{IN} = 2V_{OUT}$, (Figure 1 circuit).

A graph for selecting C_T vs frequency including the effects of input voltage is given in Figure 3.

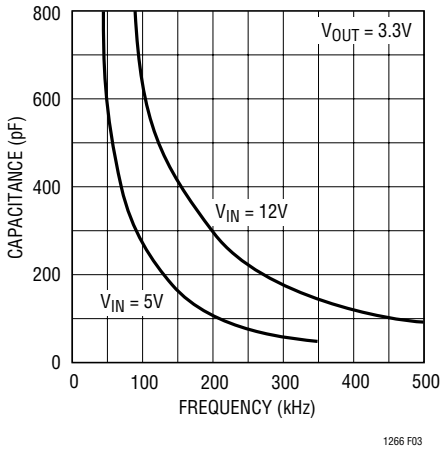


Figure 3. Timing Capacitor Value

APPLICATIONS INFORMATION

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \bullet 10^4 \bullet C_T \bullet \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $25mV/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \bullet 10^5 \bullet R_{SENSE} \bullet C_T \bullet V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1266 series may not enter Burst Mode operation and efficiency will be slightly degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using ferrite, Kool Mμ® on molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ is a very good, low loss core material for toroids, with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequency. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corp. which do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1266 series: either a P-channel MOSFET or an N-channel MOSFET for the main switch and an N-channel MOSFET for the synchronous switch. The main selection criteria for the power MOSFETs are the type of MOSFET, threshold voltage $V_{GS(TH)}$ and on-resistance $R_{DS(ON)}$.

The cost and maximum output current determine the type of MOSFET for the topside switch. N-channel MOSFETs have the advantage of lower cost and lower $R_{DS(ON)}$ at the expense of slightly increased circuit complexity. For lower current applications where the losses due to $R_{DS(ON)}$ are small, a P-channel MOSFET is recommended due to the lower circuit complexity. However, at load currents in excess of 3A where the $R_{DS(ON)}$ becomes a significant portion of the total power loss, an N-channel is strongly recommended to maximize efficiency.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1266 series is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the two MOSFETs are given by:

$$\text{Topside Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom-Side Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

Kool Mμ is a registered trademark of Magnetics, Inc.

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From the duty cycles, the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$TS\ R_{DS(ON)} = \frac{V_{IN} \bullet P_T}{V_{OUT} \bullet I_{MAX}^2 \bullet (1 + \delta_T)}$$

$$BS\ R_{DS(ON)} = \frac{V_{IN} \bullet P_B}{(V_{IN} - V_{OUT}) \bullet I_{MAX}^2 \bullet (1 + \delta_B)}$$

where P_T and P_B are the allowable power dissipations and δ_T and δ_B are the temperature dependencies of $R_{DS(ON)}$. P_T and P_B will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). For a MOSFET, $(1 + \delta)$ is generally given in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta_{PCH} = 0.007/°C$ and $\delta_{NCH} = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For $V_{IN} > 8V$, standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5V$) are strongly recommended. The LTC1266 series Power V_{IN} must always be less than the absolute maximum V_{GS} ratings for the MOSFETs.

The Schottky diode D1 shown in Figure 1 only conducts during the deadtime between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the bottom-side MOSFET from turning on and storing charge during the deadtime, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the current through the topside MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR (Effective Series Resistance) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ Required\ I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on Power V_{IN} (Pin 2) for high frequency decoupling.

The selection of C_{OUT} is driven by the required ESR. *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1266 series:*

$$C_{OUT}\ Required\ ESR < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent. If Burst Mode operation is disabled, the ESR requirement can be relaxed and is limited only by the allowable output voltage ripple.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirements of the application. An excellent choice is the AVX TPS series of surface mount tantalums.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1266

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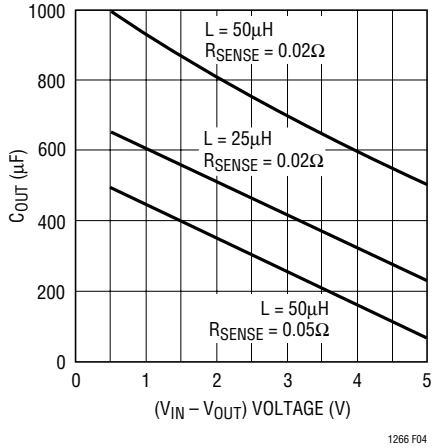

Figure 4. Minimum Value of C_{OUT}

series would normally be in continuous operation. The output remains in regulation at all times. This minimum capacitance requirement may be relaxed if Burst Mode operation is disabled.

N-Channel vs P-Channel MOSFETs

The LTC1266 has the capability to drive either an N-channel or a P-channel topside switch to give the user more flexibility. N-channel MOSFETs are superior in performance to P-channel due to their lower $R_{DS(ON)}$ and lower gate capacitance and are typically less expensive; however, they do have a slightly more complicated gate drive requirement and a more limited input voltage range (see following sections).

Driving P-Channel Topside MOSFETs

The P-channel topside switch circuit configuration is the most straightforward due to the requirement of only one supply voltage level. This is due to the negative gate threshold of the P-channel MOSFET which allows the MOSFET to be switched on and off by swinging the gate between V_{IN} and ground. The phase invert (Pin 3) is tied to ground to choose this operating mode. Normally, the converter input (V_{IN}) is connected to the LTC1266 supply Pins 2 and 5 and can go as high as 20V. Pin 2 supplies the high frequency current pulses to switch the MOSFETs and should be decoupled with a 0.1µF to 1µF ceramic capacitor. Pin 5 supplies most of the quiescent power to the rest of the chip.

Driving N-Channel Topside MOSFETs

Driving an N-channel topside MOSFET (PINV, Pin 3, tied to PWR V_{IN}) is a little trickier than driving a P-channel since the gate voltage must be positive with respect to the source to turn it on, which means that the gate voltage must be higher than V_{IN}. This requires either a second supply at least $V_{GS(ON)}$ above V_{IN} or a bootstrapping circuit to boost the V_{IN} to the proper level. The easiest method is using a higher supply (see Figure 14) but if one is not available, the bootstrap method can be used at the expense of an additional diode (see Figure 1). The bootstrap works by charging the bootstrap capacitor to V_{IN} during the off-time. During the on-time, the bottom plate of the capacitor is pulled up to V_{IN} so that the voltage at Pin 2 is now twice V_{IN} (plus any ringing on the switch node).

Since the maximum allowable voltage at Pin 2 is 20V, the Figure 1 bootstrap circuit limits V_{IN} to less than 10V. A higher V_{IN} can be achieved if the bootstrap capacitor is charged to a voltage less than V_{IN}, in which case $V_{IN(MAX)} = 20 – V_{CAP}$.

N-channel mode, internal circuitry limits the maximum on-time to 60µs to guarantee start-up of the bootstrap circuit. This maximum on-time reduces the maximum duty cycle to:

$$\text{Max Duty Cycle} = \frac{60\mu s}{60\mu s + t_{OFF}}$$

which slightly increases the minimum input voltage at which dropout occurs. However, because of the superior on-conductance of the N-channel, the dropout performance of an all N-channel regulator is still better (see Figure 5) even with the duty cycle limitation, except at light loads.

Low-Battery Comparator

The LTC1266 has an on-chip low-battery comparator which can be used to sense a low-battery condition when implemented as shown in Figure 6. The resistor divider R1, R2 sets the comparator trip point as follows:

$$V_{TRIP} = 1.25\left(1 + \frac{R2}{R1}\right)$$

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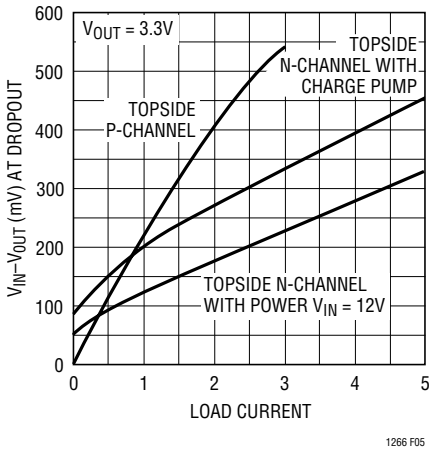

Figure 5. Comparison of Dropout Performance

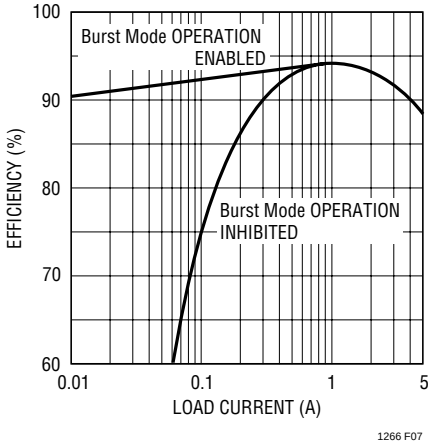

Figure 7. Effect of Disabling Burst Mode Operation on Efficiency

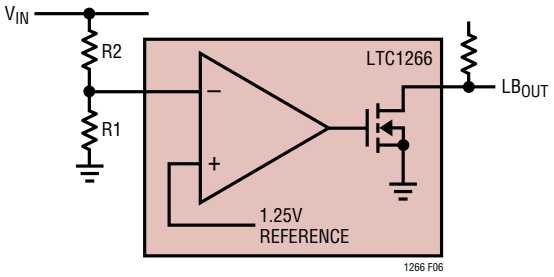

Figure 6. Low-Battery Comparator

The divided down voltage at the "–" input to the comparator is compared to an internal 1.25V reference. This reference is separate from the 1.265V reference used by the voltage comparator and current comparator for regulation and is not disabled by the shutdown pin, therefore the low-battery detection is operational even when the rest of the chip is shut down. The comparator is functional down to an input voltage of 2.5V. Thus, the output will provide a valid state even when the rest of the chip does not have sufficient voltage to operate. For best performance, the value of the pull-up resistor should be high enough that the output is pulled down to ground when sinking 200µA or less.

Suppressing Burst Mode Operation

Normally, enabling Burst Mode operation is desired due to its superior efficiency at low load currents (see Figure 7).

However, in certain applications it may be desirable to inhibit this feature. Some reasons for doing so are:

1. To eliminate audible noise from certain types of inductors at light loads.

2. If the load is never expected to drop low enough to benefit from the efficiency advantages of Burst Mode operation, the output capacitor ESR and minimum capacitance requirements (which may falsely trigger Burst Mode operation if not met) can be relaxed if Burst Mode operation is disabled.

3. If an auxiliary winding is used. Disabling Burst Mode operation guarantees switching independent of the load on the primary. This allows power to be taken from the auxiliary winding independently.

4. Tighter load regulation (< 1%).

Burst Mode operation is disabled by applying a CMOS logic high voltage (>2.1V) to Pin 4. When it is disabled, the voltage comparator limit is raised high enough so that it no longer is involved in regulation; however it is still active and is useful as a voltage clamp to keep the output from overshooting.

Note that since the inductor current must reverse to regulate the output at zero load when Burst Mode operation is disabled, the minimum inductance (L_{MIN}) specified during Inductor Core Selection is no longer applicable.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or

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discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The Pin 7 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits, only small errors are incurred by expressing losses as a percentage of output power).

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC1266 series circuits: 1) LTC1266 DC bias current, 2) MOSFET gate charge current and 3) I^2R losses.

1. The DC supply current is the current which flows into V_{IN} (Pin 2). For V_{IN} = 10V the LTC1266 DC supply current is 170μA for no load, and increases proportionally with load up to a constant 2.1mA after the LTC1266 series has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 5V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from Power V_{IN} to ground. The resulting dQ/dt is a current flowing into Power V_{IN} (Pin 5) which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f (Q_N + Q_P)$. The typical gate charge for a 0.05Ω N-channel power MOSFET is 15nC. This results in $I_{GATECHG}$ = 6mA in 200kHz continuous operation for a 2% to 3% typical mid-current loss with V_{IN} = 5V.

Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside and bottom-side MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.05Ω, R_L = 0.05Ω and R_{SENSE} = 0.02Ω, then the total resistance is 0.12Ω. This results in losses ranging from 3.5% to 15% as the output current increases from 1A to 5A. I^2R losses cause the efficiency to roll off at high output currents.

Figure 8 shows how the efficiency losses in a typical LTC1266 series regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels (see Figure 7). With Burst Mode

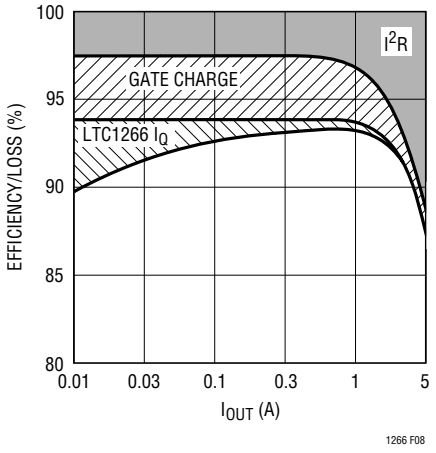

Figure 8. Efficiency Loss

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operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected the I^2R losses dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during deadtime and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 5V (nominal), V_{OUT} = 3.3V, I_{MAX} = 5A and f = 200kHz; R_{SENSE}, C_T and L can immediately be calculated:

$R_{SENSE} = 100mV/5 = 0.02\Omega$

$t_{OFF} = (1/200kHz) \bullet [1 – (3.3/5)] = 1.7\mu s$

$C_T = 1.7\mu s/(1.3 \bullet 10^4) = 130pF$

$L_{MIN} = 5.1 \bullet 10^5 \bullet 0.02\Omega \bullet 130pF \bullet 3.3V = 5\mu H$

Assume that the MOSFET dissipations are to be limited to $P_T = P_B = 2W$.

If T_A = 40°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 140°C and $\delta_T = \delta_B = 0.60$. The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$TS\ R_{DS(ON)} = \frac{5(2)}{3.3(5)^2\ (1.60)} = 0.076\Omega$$

$$BS\ R_{DS(ON)} = \frac{5(2)}{1.7(5)^2\ (1.60)} = 0.147\Omega$$

The topside FET requirement can be met by an N-channel Si9410DY which has an $R_{DS(ON)}$ of about 0.04Ω at V_{GS} = 5V. The bottom-side FET requirement is exceeded by an Si9410DY. Note that the most stringent requirement for the bottom-side MOSFET is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst-case dissipation rises to:

$P_B = I_{SC(AVG)}{}^2 \bullet R_{DS(ON)} \bullet (1 + \delta_B)$

With the 0.02Ω sense resistor, $I_{SC(AVG)} \approx 6A$ will result, increasing the 0.04Ω bottom-side FET dissipation to 2.3W. C_{IN} will require an RMS current rating of at least 2.5A at temperature and C_{OUT} will require an ESR of 0.02Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. The minimum V_{IN} can be calculated from the maximum duty cycle and voltage drop across the topside FET,

$$V_{MIN} = \frac{V_{OUT} + I_{LOAD} \bullet (R_{DS(ON)} + R_L + R_{SENSE})}{D_{MAX}} = 4.0V$$

At this lower input voltage, the operating frequency decreases and the topside FET will be conducting most of the time, causing the power dissipation to increase. At dropout,

$$f_{MIN} = \frac{1}{t_{ON\ (MAX)} + t_{OFF}} = 16kHz$$

$P_T = I^2_{LOAD} \bullet R_{DS(ON)} \bullet (1 + \delta_T) \bullet D_{MAX}$

This last step is necessary to assure that the power dissipation and junction temperature of the topside FET are not exceeded.

These last calculations assume that Power V_{IN} is high enough to keep the topside FET fully turned on at dropout, as would be the case with the Figure 11circuit. If this isn't true (as with the Figure 1 circuit) the $R_{DS(ON)}$ will increase which in turn increases V_{MIN} and P_T.

Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1266 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB}, Pin 10. The regulated voltage is determined by:

$$V_{OUT} = 1.265\left(1 + \frac{R2}{R1}\right)$$

To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1266.

For Figure 1 applications with V_{OUT} below 2V, or when R_{SENSE} is moved to ground, the current sense comparator inputs operate near ground. When the current comparator is operated at less than 2V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

APPLICATIONS INFORMATION

Troubleshooting Hints

Since efficiency is critical to LTC1266 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor, Pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation should occur with the C_T pin waveform periodically falling to ground for periods of time as shown in Figure 9b.

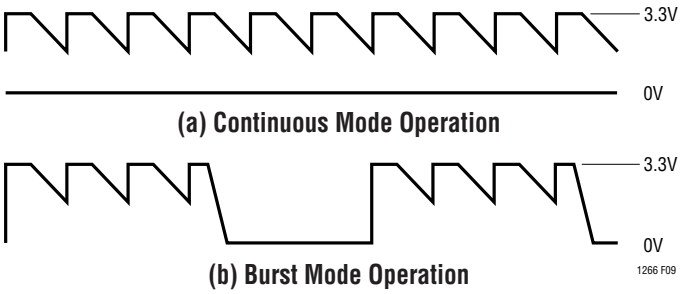


Figure 9. C_T Waveforms

If Pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1266 series. These items are also illustrated graphically in the layout diagram of Figure 10. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1266 signal ground (Pin 12) must return to the (–) plate of C_{OUT}. The power ground returns to the source of the bottom-side MOSFET, anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible.

2. Does the LTC1266 SENSE$^-$ (Pin 8) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.

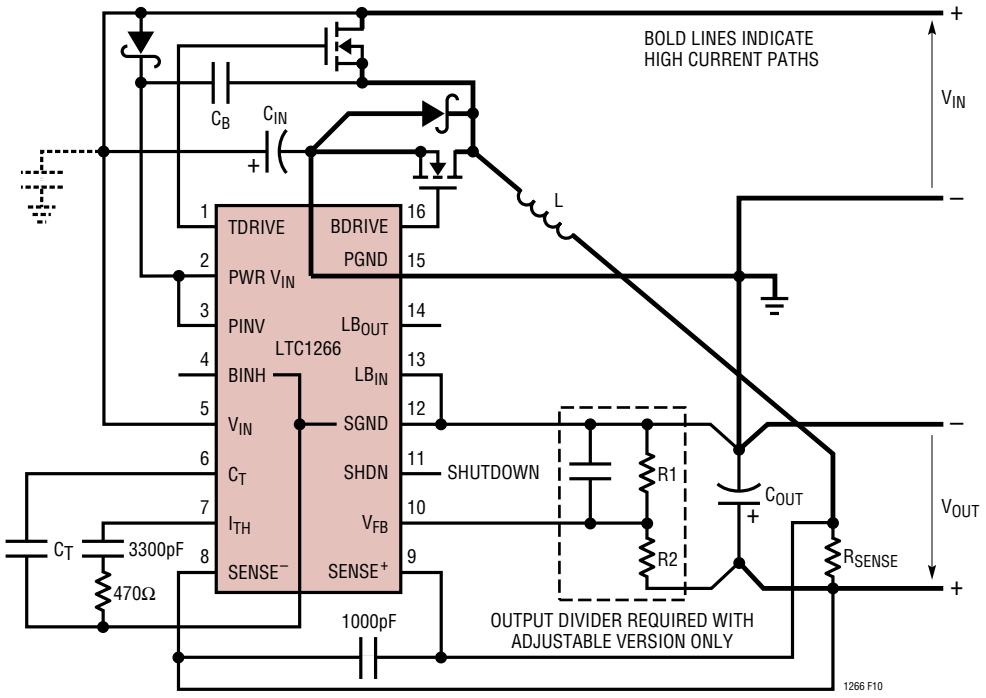


Figure 10. LTC1266 Layout Diagram (See Layout Checklist)

APPLICATIONS INFORMATION

3. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 8 and 9 should be as close as possible to the LTC1266.

4. Does the (+) plate of C_{IN} connect to the source of the topside MOSFET as closely as possible? This capacitor provides the AC current to the topside MOSFET.

5. A 0.1µF to 1µF decoupling capacitor connected between V_{IN} (Pin 5) and ground is optional, but is sometimes helpful in eliminating instabilities at high input voltage and high output loads.

6. Is the shutdown (Pin 11) actively pulled to ground during normal operation? The shutdown pin is high impedance and must not be allowed to float. The select (Pins 3 and 4) are also high impedance and must be tied high or low depending on the application.

TYPICAL APPLICATIONS (Layout Assist Schematics)

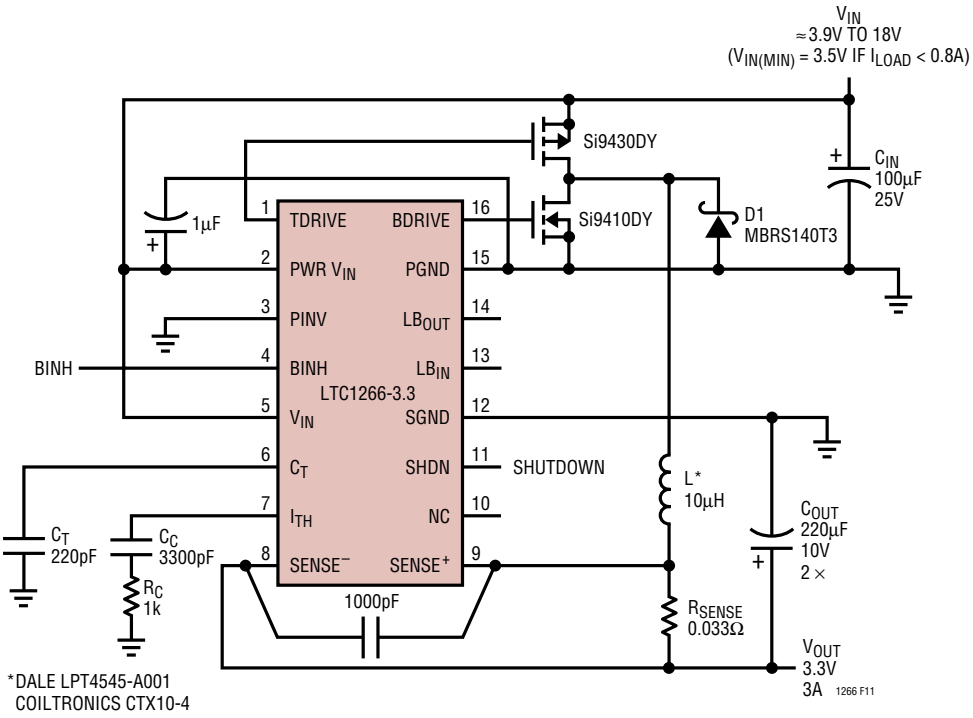


Figure 11. Low Dropout, 3.3V/3A High Efficiency Regulator

TYPICAL APPLICATIONS (Layout Assist Schematics)

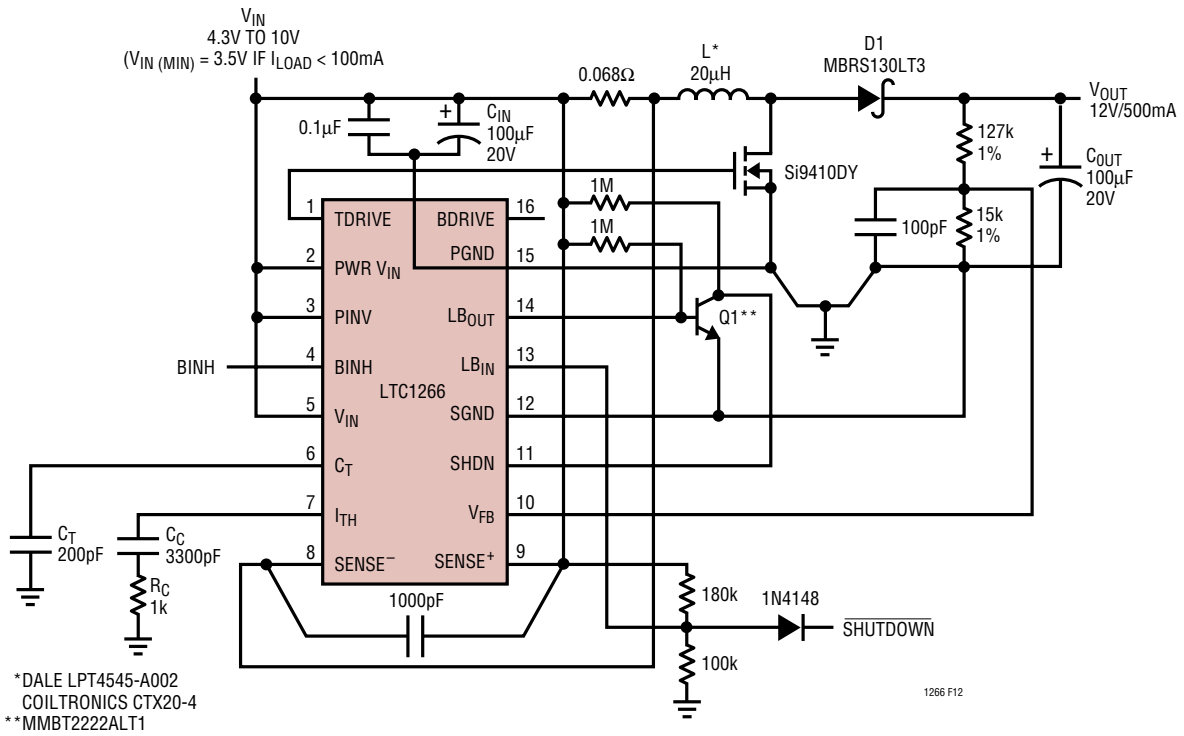


Figure 12. 5V to 12V/500mA High Efficiency Boost Regulator

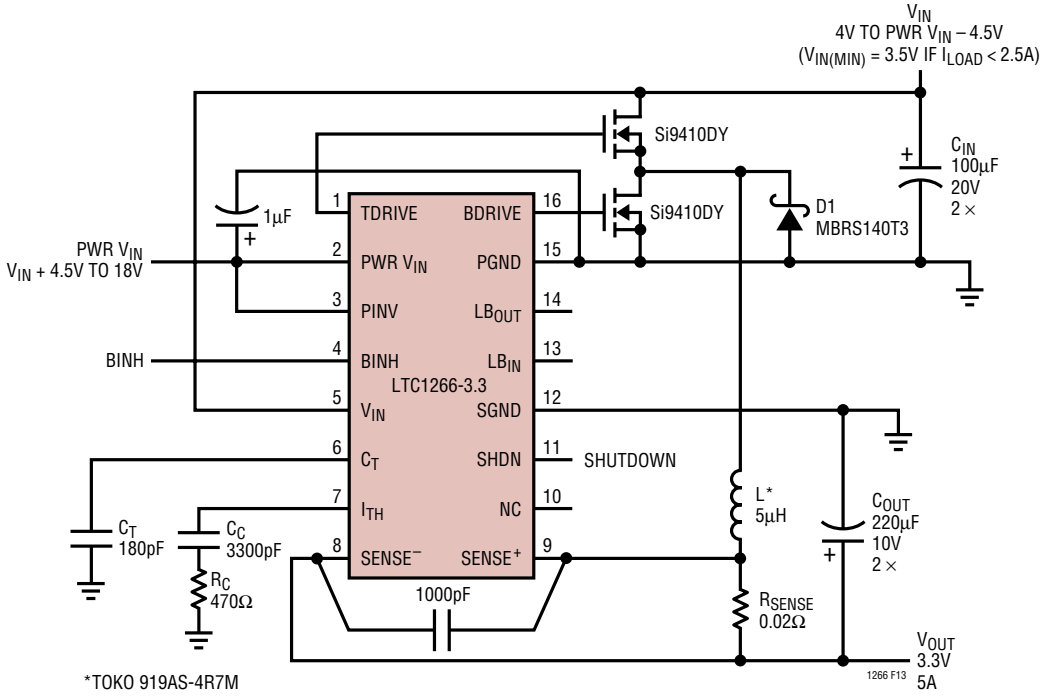


Figure 13. All N-Channel 5V to 3.3V/5A Converter with Drivers Powered from External PWR V_{IN} Supply

TYPICAL APPLICATIONS (Layout Assist Schematics)

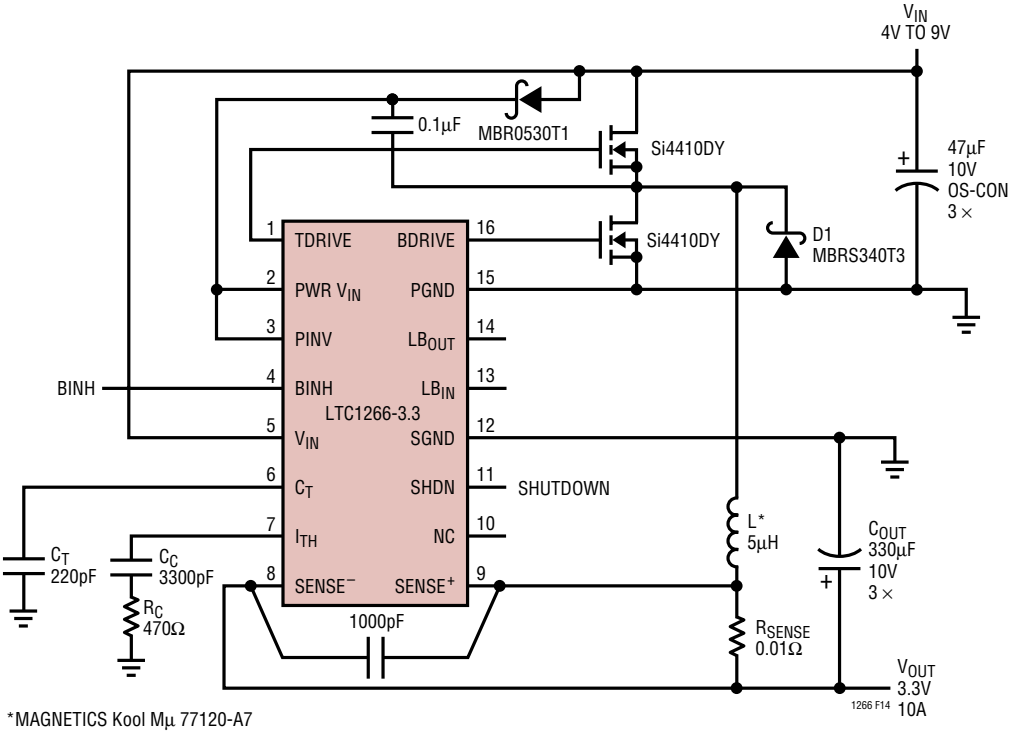


Figure 14. All N-Channel 5V to 3.3V/10A High Efficiency Regulator

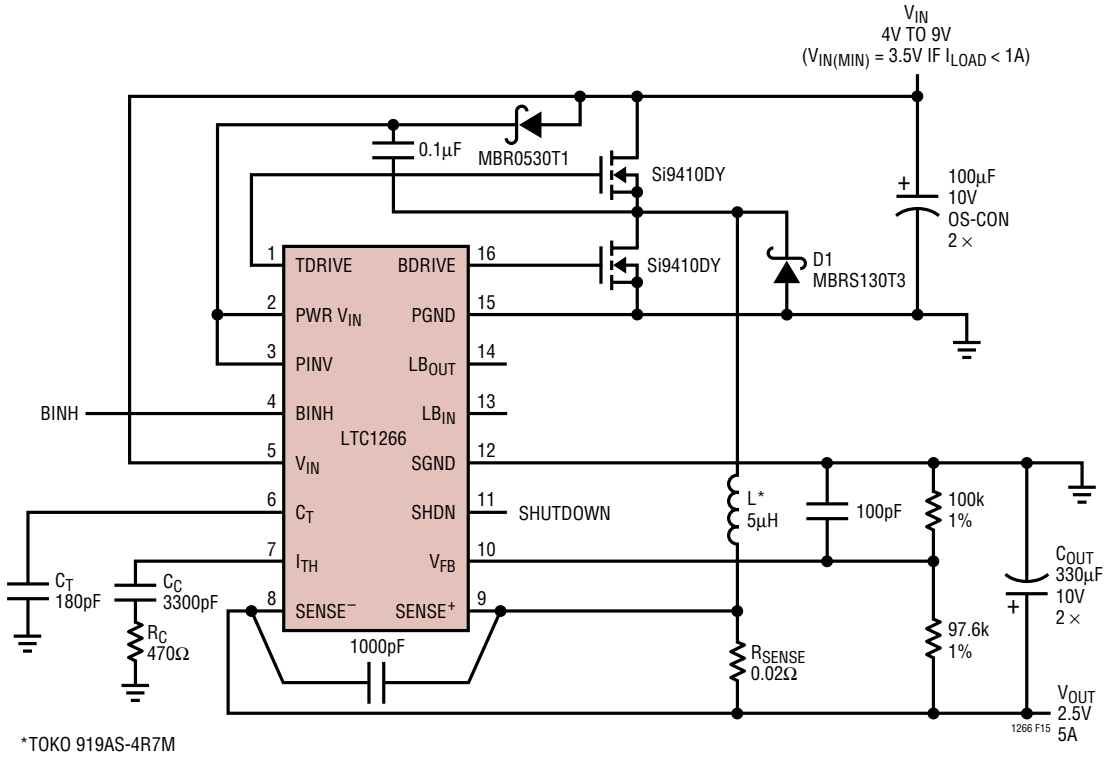
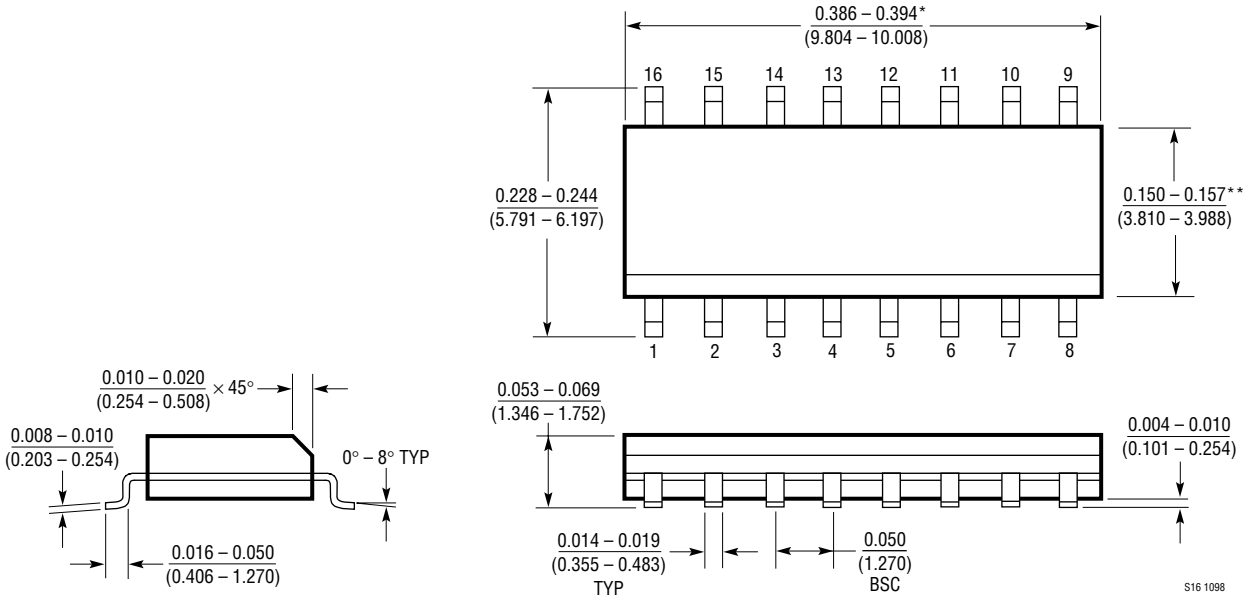


Figure 15. All N-Channel 5V to 2.5V/5A High Efficiency Regulator

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1530	Synchronous Step-Down Controller in SO-8	No R_{SENSE}™ Voltage Mode, I_{OUT} Up to 15A
LTC1625	97% Efficiency Synchronous Step-Down Controller	No R_{SENSE} Current Mode, Low Dropout, I_{OUT} Up to 20A, V_{OUT} Up to 36V
LTC1628	2-Phase, Dual Synchronous Controller	Minimizes C_{IN} and C_{OUT}, Two Outputs $4V \le V_{IN} \le 36V$, I_{OUT} Up to 20A
LTC1735	High Efficiency Synchronous Controller	Wide Input Range $3.5V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 6V$ OPTI-LOOP™ Compensation Minimizes C_{OUT}
LTC1772	SOT-23 P-Channel Controller	Tiny Design, 550kHz, $2.5V \le V_{IN} \le 9.8V$, I_{OUT} Up to 4.5A
LTC1929	42A 2-Phase Synchronous Controller for Single Output	I_{OUT} Up to 42A with Single Controller, Minimizes C_{IN} and C_{OUT}, Up to 200A Out

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