

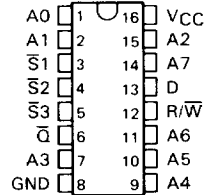
# SN74S201, SN74S301 256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

D2007, SEPTEMBER 1977—FEBRUARY 1984

## STATIC RANDOM-ACCESS MEMORIES

- Static Fully Decoded RAM's Organized as 256 Words of One Bit Each
- Schottky-Clamped for High Performance
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I<sup>2</sup>L Circuits
- Chip-Select Input Simplify External Decoding
- Typical Performance:  
     Read Access Time . . . 42 ns  
     Power dissipation . . . 500 mW

SN74S201, SN74S301 . . . J OR N PACKAGE  
(TOP VIEW)



### description

These 256-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of one bit. They are fully decoded and have three chip-select inputs to simplify decoding required to achieve expanded system organizations.

### write cycle

The information applied at the data input is written into the selected location when the chip-select inputs and the write-enable input are low. While the write-enable input is low, the 'S201 outputs are in the high-impedance state and the 'S301 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

### read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three chip-select inputs is low. When any one of the chip-select inputs are high, the 'S201 outputs will be in the high-impedance state and the 'S301 outputs will be off.

FUNCTION TABLE

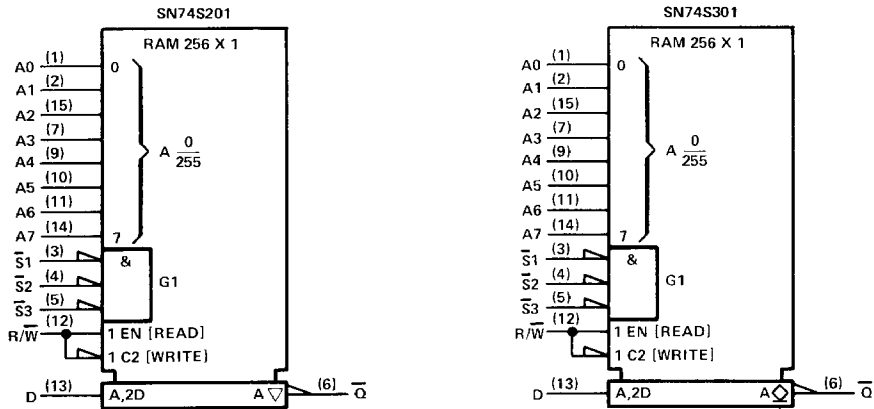
FUNCTION	INPUTS		'S201 OUTPUT ( $\bar{Q}$ )	'S301 OUTPUT ( $\bar{Q}$ )
	CHIP SELECT $\bar{S}$	WRITE ENABLE R/W		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant  
 For chip-select: L = all  $\bar{S}_i$  inputs low, H = one or more  $\bar{S}_i$  inputs high

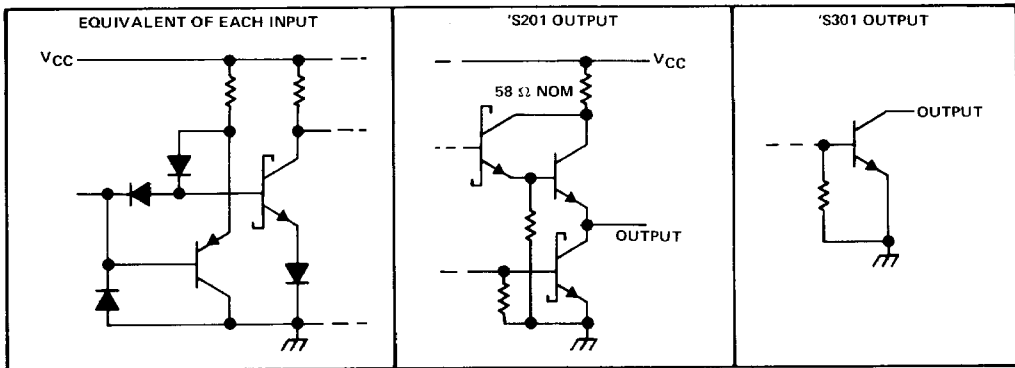
5  
RAMs

# SN74S201, SN74S301 256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

## logic symbols



## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Off-State output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

**5**  
**RAMS**

# SN74S201, SN74S301 256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

## recommended operating conditions

		SN74S201			SN74S301			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)		4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, $V_{OH}$					5.5			V
High-level output current, $I_{OH}$					-10.3			mA
Low-level output current, $I_{OL}$					16			mA
Width of write pulse (write enable low), $t_w(wr)$		65			65			ns
Setup time	Address before write pulse, $t_{su}(ad)$	0†			0†			ns
	Data before end of write pulse, $t_{su}(da)$	65†			65†			
	Chip select before end of write pulse, $t_{su}(\bar{S})$	65†			65†			
Hold time	Address after write pulse, $t_h(ad)$	0†			0†			ns
	Data after write pulse, $t_h(da)$	0†			0†			
	Chip-select after write pulse, $t_h(\bar{S})$	0†			0†			
Operating free-air temperature, $T_A$		0			70			°C

† The arrow indicates the transition of the write-enable input used for reference: ↓ for the low-to-high transition, ↓ for the high-to-low transition.  
NOTE 1: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	'S201			'S301			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage		0.8			0.8			V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.2			-1.2			V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = \text{MAX}$	2.4						V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$	0.45			0.45			V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OL} = 2.4 \text{ V}$				40			μA
	$V_{IL} = 0.8 \text{ V}, V_{OL} = 5.5 \text{ V}$				100			
$I_{OZH}$ Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 2.4 \text{ V}$	40						μA
$I_{OZL}$ Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OL} = 0.5 \text{ V}$	-40						μA
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	25			25			μA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$	-250			-250			μA
$I_{OS}$ Short-circuit output current §	$V_{CC} = \text{MAX}$	-30	-100				mA	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	100	140		100	140	mA	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with all chip-select inputs grounded, all other inputs at 4.5 V, and the output open.

**5**  
**RAMs**

**SN74S201, SN74S301**  
**256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES**

**'S201 switching characteristics over recommended operating ranges of  $T_A$  and  $V_{CC}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
$t_{a(ad)}$	Access time from address	$C_L = 30$ pF, See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip select (select time)			13	30	ns
$t_{SR}$	Sense recovery time			20	40	ns
$t_{PXZ}$	Disable time from high or low level	From $\bar{S}$	$C_L = 5$ pF, See Note 3	9	20	ns
		From $R/\bar{W}$				

**'S301 switching characteristics over recommended operating ranges of  $T_A$  and  $V_{CC}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
$t_{a(ad)}$	Access time from address	$C_L = 30$ pF, $R_{L1} = 300$ $\Omega$ , $R_{L2} = 600$ $\Omega$ , See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip enable (enable time)			13	30	ns
$t_{SR}$	Sense recovery time			20	40	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output (disable time)	From $\bar{S}$		8	20	ns
		From $R/\bar{W}$				
				15	35	

<sup>‡</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ$ .

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**5**

**RAMS**