(13) 103533

1.0 General Description

National Semiconductor's CMOS gate array Family utilizes a dual layer metal technology (microCMOS) to achieve operating speeds similar to Schottky-TTL with the inherent lower power consumption of standard CMOS integrated circuits. The SCX6200-Series Family is available in 2-micron drawn geometry with a 1.4 micron effective channel length. The range of complexity is currently from 600 to 6000 gates. The gates are arranged in cells. Each cell has the equivalent of three 2-input NAND or NOR gates. All outputs have the ability to drive 10 LSTTL loads. All inputs have high noise immunity and are protected from static discharge.

National Semiconductor supports gate array designs with a variety of user/vendor interfaces. This ranges from producing arrays from the user's schematic to accepting databases for mask generation. A large dedicated staff of gate array professionals is available to help the user determine the most efficient and cost effective way to interface on any given design.

The design automation tools include workstation or text file entry (for schematic capture), logic and timing verifiers to substantiate the actual design, fault grading analysis to gauge testability and a large selection of macros (hardware and software) to speed and simplify the design.

2.0 Product Features

- Latch-up proof, state-of-the-art 2-micron (drawn) dual-metal silicon-gate microCMOS technology
- Ultra-high performance—1 ns typical gate delays
- Available from 600 gates to 6000 gates
- CMOS power dissipation
- All inputs and I/Os protected from over-voltage and latch-up
- Full design automation support
  - — Schematic capture
  - — Logic simulator with timing information
  - — Fault grading
- Multiple power rail pin connections
- Multiple packaging options in ceramic, plastic, leaded and leadless
- Pin counts to 172
- Military performance
- Alternately sourced
- Complete hardware/software macrocell libraries
- On-chip self-test capability (6.0K only)
- 100% auto-place-and-route at 90% utilization
- Design automation system supported on mainframe and workstations

2.0.1 Enhanced Product Features

The SCX6200-series gate array family is available in seven device increments from 600 to 6000 gates. The initial members of the 2-micron family consist of SCX6212, 6225 and 6260. Today it has been enhanced and expanded to include the 6244, 6232, 6218 and 6206. These enhanced devices contain several new features as follows:

- **Flexible I/O Structure** - The I/O buffer has been enhanced to handle multiple functions including:
  - — Low-drive inputs compatible with TTL, CMOS or Schmitt Trigger
  - — High-drive (Clock Driver) inputs compatible with TTL, CMOS or Schmitt Trigger
  - — Output compatible with TTL and CMOS and configurable as TRI-STATE®, non TRI-STATE or Open Drain
  - — Outputs selectable for 1, 2 or 4 mA drive
  - — Bidirectional inputs/outputs
  - — Oscillator macros to drive 1, 2 or 4 mA
  - — Separate power supply traces for output drivers improve noise immunity

The input capacitance loading of the output drivers has also been reduced to enhance the overall circuit performance.

- **Selectable Output Drive Capability** - The enhanced I/O structure now makes it possible to offer a variety of output drives for any given I/O location. Through implementation of I/O macro options, users can select their output drives in 1, 2 or 4 mA for each output buffer.
- **Parallel I/O Buffers for High Drives** - By means of special I/O macros, output drive current in excess of 4 mA can be achieved by paralleling I/O buffers without losing the input functions. For example, to achieve 24 mA, six 4 mA I/O buffers need to be paralleled up; through use of the special macros, one pin is needed to implement the output which can be bidirectional while 5 pins can still be used as inputs.
- **Dedicated Multiplexed D-Flip/Flops** - Incorporated into the internal array core is a number of dedicated multiplexed D-flip/flops. These flip/flops have been designed to achieve significant system speed improvement over a logically eqivalent macro function while minimizing silicon space to implement. They are ideal for scan path design techniques as well as registers and counters.

Array Name	Equivalent 2-Input Gates (Note 1)	Input Cells	I/O Cells	Signal Pins	Test Pin	V_{DD} Pins	V_{SS} Pins
SCX6206	600	8	40	48	1	4	4
SCX6212	1260	17	42	59	1	4	4
SCX6218	1806	3	70	73	1	8	8
SCX6225	2430	12	76	88	1	6	6
SCX6232	3162	3	101	104	1	8	8
SCX6244	4380	3	110	113	1	8	8
SCX6260 (Note 2)	6090	66	88	154	6	8	8

Note 1: Input and I/O cells are not considered part of the internal cell count.

Note 2: Advanced Architecture with additional 2500 gates for on-chip self-test capability.

7.0 Packaging

The SCX family of microCMOS gate arrays is offered in a very wide variety of packages. The user is provided with many choices in terms of both package type and lead count. The package types offered include ceramic pin grid arrays (PGA), leaded ceramic chip carriers (LDCC), leadless ceramic chip carriers (LCC), plastic leaded chip carriers (PCC), ceramic DIPs, and plastic DIPs.

The availability of such a large variety of packages gives the user flexibility in making the following choices:

—Ceramic versus plastic

—Through-hole mount versus surface mount

The specific packages offered are listed in Table IVa.

Surface mounting of multi-lead components is rapidly gaining popularity. To provide the user flexibility, National Semiconductor offers its CMOS gate arrays in several surface mount package options: leaded and leadless ceramic chip carrier and the plastic leaded chip carrier.

Surface mounting refers to component attachment, whereby the component leads or pads rest on the surface of the PCB instead of the traditional approach of inserting the leads into through-holes which go through the board. With surface mounting there are solder pads on the PCB which align with the leads or pads on the component. The resulting solder joint forms both the mechanical and electrical connections.

The primary reason for surface mounting is to allow leads to be placed closer together than the 0.100 inch standard for DIPs with through-hole mounting. Through-hole mounting on smaller than 0.100 inch space is difficult to achieve in production and is generally avoided. The move to 0.050 inch lead spacing offered with the current generation of surface mounted components, along with a switch from a dual-in-line format to a quad format, has achieved a threefold increase in component mounting density. A need to achieve greater density is a major driving force in today's marketplace.

Learning how to surface mount components to printed circuit boards requires the user to implement an assembly process not typically associated with through-hole insertion/wave soldering assembly methods.

Surface mounting involves three basic process steps:

1) Application of solder or solder paste to the printed circuit board

2) Positioning of the component onto the printed circuit

3) Reflowing of the solder or solder paste.

Table IVb lists the manufacturers currently offering sockets for each of the advanced package options listed in this data sheet. A matrix of which manufacturers to contact for each socket option is provided. The listing is divided into test/burn-in and production categories. There may be some individual sockets that will cover both requirements.

TABLE IVa. Gate Array Package Options

Package Type	Pins	6206	6212	6218	6225	6232	6244	6260
Plastic DIP, N	20	X						
	28	X	X	X	X			
	40	X	X	X	X	X	X	
	48	X	X	X	X	X	X	
Ceramic DIP, D (Side Braze)	20	X						
	28	X	X	X	X			
	40	X	X	X	X	X	X	
	48	X	X	X	X	X	X	
Plastic Leaded Chip Carrier, PCC	28	X	X	X	X			
	44	X	X	X	X	X	X	
	68		X	X	X	X	X	
	84			X	X	X	X	
	124				X	X	X	
Ceramic Leaded Chip Carrier, LDCC	124				X	X	X	X
Ceramic Leadless Chip Carrier, LCC	28	X	X	X	X			
	44	X	X	X	X	X		
	68		X	X	X	X	X	
	84			X	X	X	X	
	124				X	X	X	X
Ceramic Pin Grid Array, PGA	68		X	X	X	X	X	
	84			X	X	X	X	
	124				X	X	X	X
	172							X