

## 32K x 8 Static RAM

### Features

- High speed
  - 10 ns
- Fast  $t_{DOE}$
- CMOS for optimum speed/power
- Low active power
  - 467 mW (max, “L” version)
- Low standby power
  - 0.275 mW (max, “L” version)
- 2V data retention (“L” version only)
- Easy memory expansion with CE and OE features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

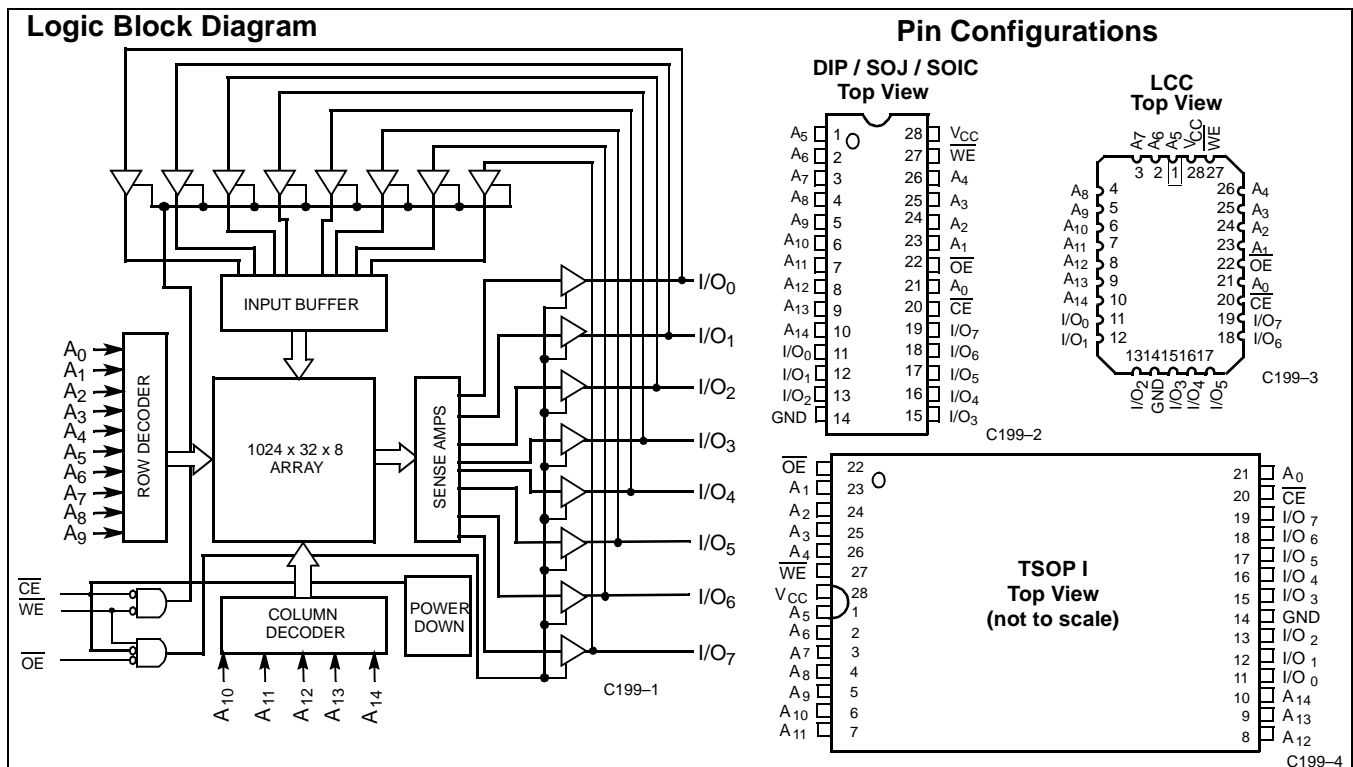
### Functional Description

The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is

provided by an active LOW Chip Enable ( $\overline{CE}$ ) and active LOW Output Enable ( $\overline{OE}$ ) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW Write Enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>14</sub>). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ( $\overline{WE}$ ) is HIGH. A die coat is used to improve alpha immunity.



### Selection Guide

	7C199-8	7C199-10	7C199-12	7C199-15	7C199-20	7C199-25	7C199-35	7C199-45
Maximum Access Time (ns)	8	10	12	15	20	25	35	45
Maximum Operating Current (mA)		120	110	160	155	150	140	140
	L		90	90	90	80	70	
Maximum CMOS Standby Current (mA)		0.5	0.5	10	10	10	10	10
	L		0.05	0.05	0.05	0.05	0.05	

Shaded area contains advance information.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14) .....	-0.5V to +7.0V

## DC Voltage Applied to Outputs

in High Z State <sup>[1]</sup> .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage <sup>[1]</sup> .....	-0.5V to $V_{CC} + 0.5V$
Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage .....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current.....	>200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	Test Conditions	7C199-8		7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	2.2	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-5	+5	-5	+5	-5	+5	-5	+5	µA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	µA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Com'l	120		110		160		155	mA
			L			85		85		100	mA
			Mil							180	mA
$I_{SB1}$	Automatic CE Power-Down Current—TTL Inputs	Max. $V_{CC}$ , $CE \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	Com'l	5		5		30		30	mA
			L			5		5		5	mA
$I_{SB2}$	Automatic CE Power-Down Current—CMOS Inputs	Max. $V_{CC}$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$	Com'l	0.5		0.5		10		10	mA
			L	0.05		0.05		0.05		0.05	mA
			Mil							15	mA

Shaded area contains advance information.

**Notes:**

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup> (continued)

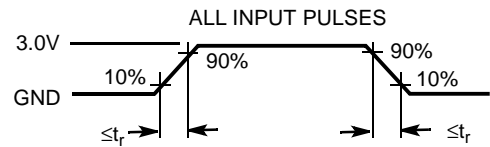
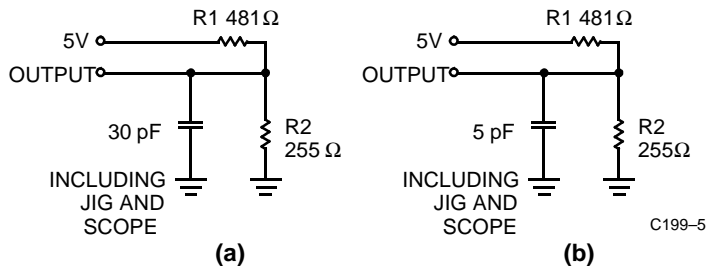
Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35		7C199-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	150		150		140		140	mA
			L	90		80		70		70	mA
			Mil	170		150		150		150	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l	30		30		25		25	mA
			L	5		5		5		5	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	10		10		10		10	mA
			L	0.05		0.05		0.05		0.05	μA
			Mil	15		15		15		15	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

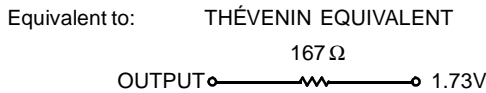
**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.

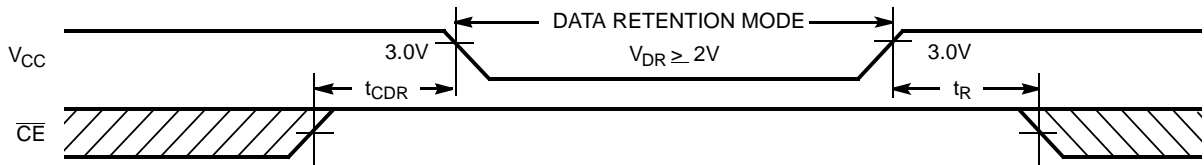
**AC Test Loads and Waveforms<sup>[5]</sup>**


C199-5

C199-6


**Data Retention Characteristics** Over the Operating Range (L version only)

Parameter	Description	Conditions <sup>[6]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'l			$\mu A$
		Com'l L		10	$\mu A$
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V$ , $CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[5]}$	Operation Recovery Time		200		$\mu s$

**Data Retention Waveform**


C199-7

**Note:**

5.  $t_R \leq 3$  ns for the -12 and the -15 speeds.  $t_R \leq 5$  ns for the -20 and slower speeds
6. No input may exceed  $V_{CC} + 0.5V$ .

**Switching Characteristics** Over the Operating Range<sup>[3, 7]</sup>

Parameter	Description	7C199-8		7C199-10		7C199-12		7C199-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
$t_{RC}$	Read Cycle Time	8		10		12		15		ns
$t_{AA}$	Address to Data Valid		8		10		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		4.5		5		5		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[8]</sup>	0		0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[8, 9]</sup>		5		5		5		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	3		3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[8, 9]</sup>		4		5		5		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		8		10		12		15	ns
<b>WRITE CYCLE</b> <sup>[10, 11]</sup>										
$t_{WC}$	Write Cycle Time	8		10		12		15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	7		7		9		10		ns
$t_{AW}$	Address Set-Up to Write End	7		7		9		10		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		7		8		9		ns
$t_{SD}$	Data Set-Up to Write End	5		5		8		9		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[9]</sup>		5		6		7		7	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	3		3		3		3		ns

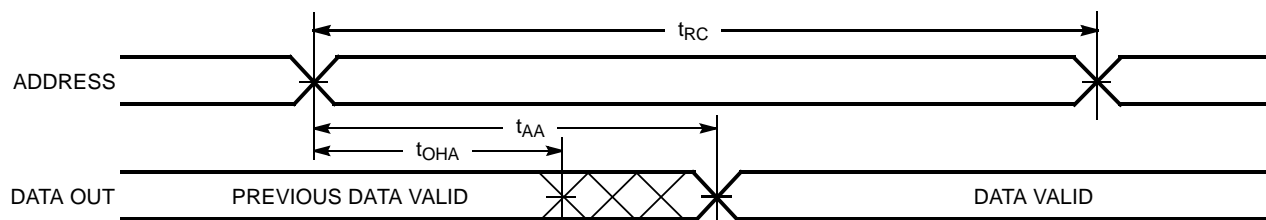
Shaded area contains advance information.

**Notes:**

7. Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
8. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
9.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Characteristics** Over the Operating Range<sup>[3,7]</sup> (continued)

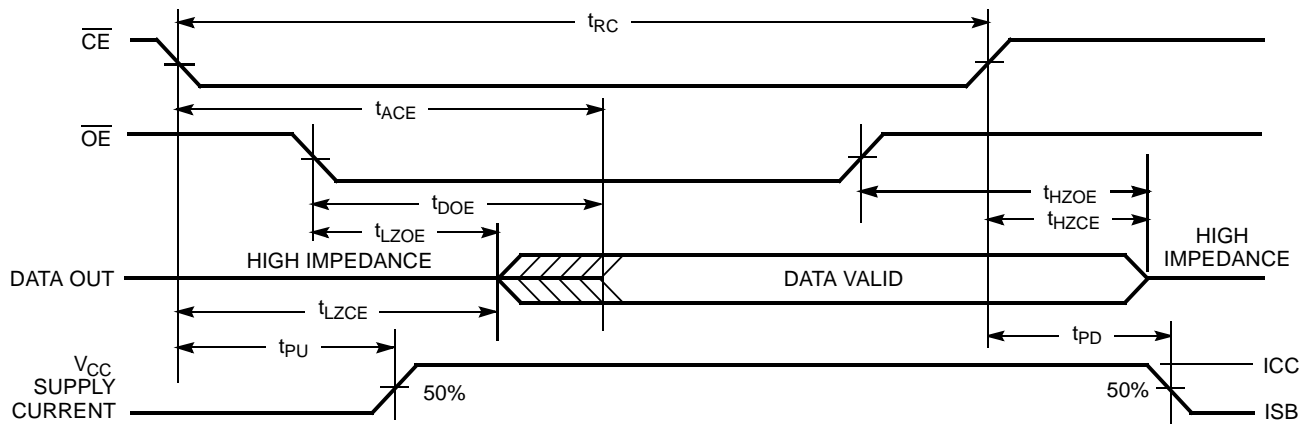
Parameter	Description	7C199-20		7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
$t_{RC}$	Read Cycle Time	20		25		35		45		ns
$t_{AA}$	Address to Data Valid		20		25		35		45	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		20		25		35		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		9		10		16		16	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[8]</sup>	0		0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[8, 9]</sup>		9		11		15		15	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[8]</sup>	3		3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[8, 9]</sup>		9		11		15		15	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		20		20		20		25	ns
<b>WRITE CYCLE</b> <sup>[10,11]</sup>										
$t_{WC}$	Write Cycle Time	20		25		35		45		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	15		18		22		22		ns
$t_{AW}$	Address Set-Up to Write End	15		20		30		40		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	15		18		22		22		ns
$t_{SD}$	Data Set-Up to Write End	10		10		15		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[9]</sup>		10		11		15		15	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[8]</sup>	3		3		3		3		ns

**Switching Waveforms**
**Read Cycle No. 1**<sup>[12, 13]</sup>


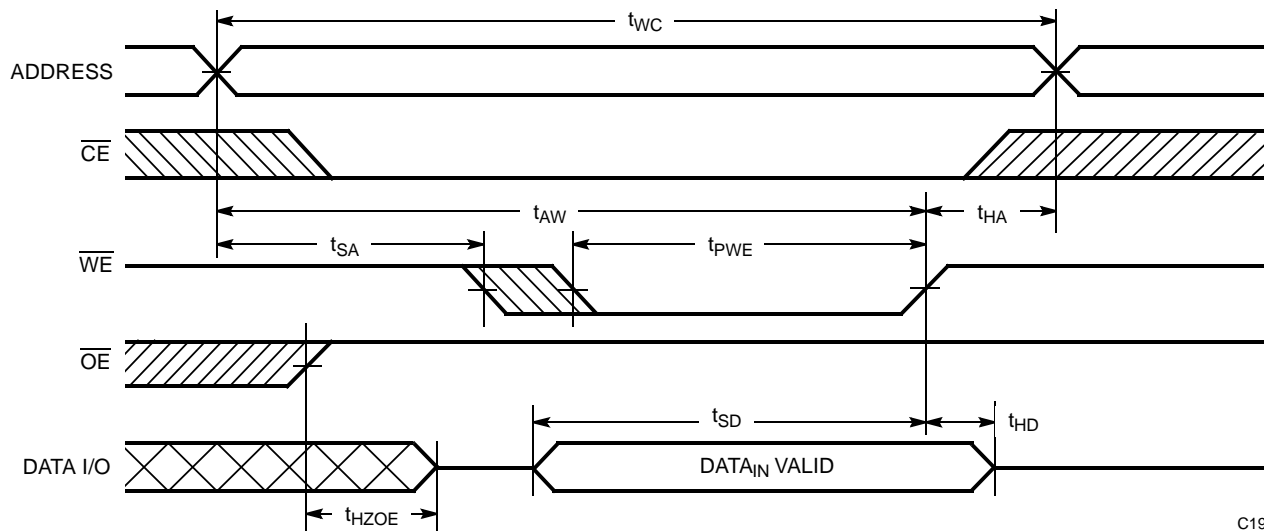
C199-8

**Notes:**

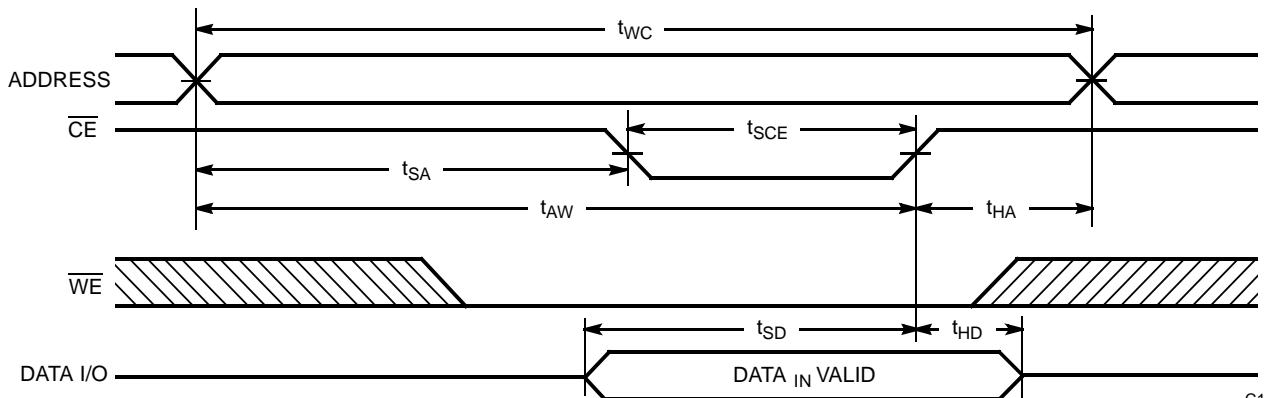
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .  
 13.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2** [13, 14]


C199-9

**Write Cycle No. 1 (WE Controlled)** [10, 15, 16]


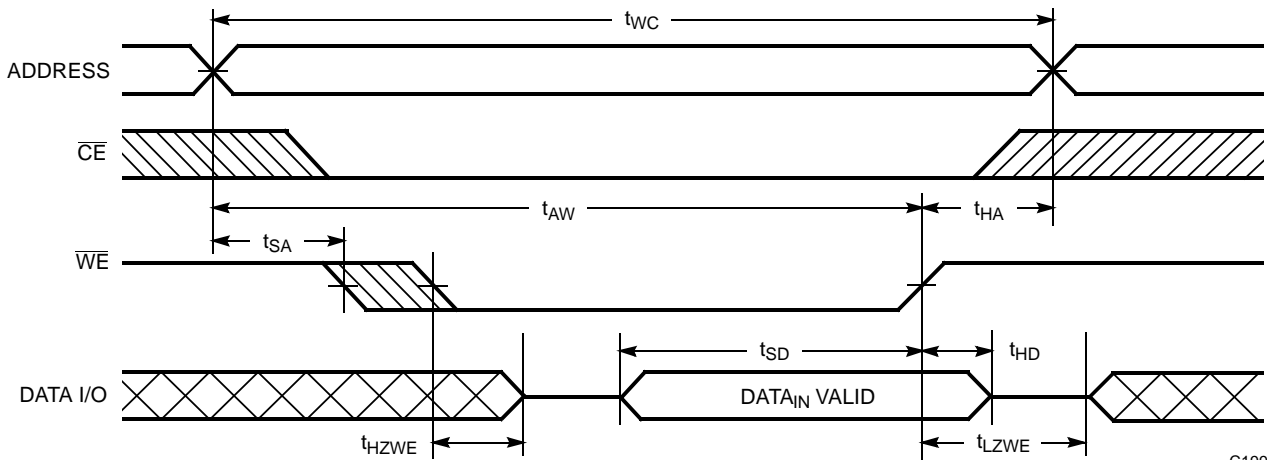
C199-10

**Write Cycle No. 2 (CE Controlled)** [10, 15, 16]


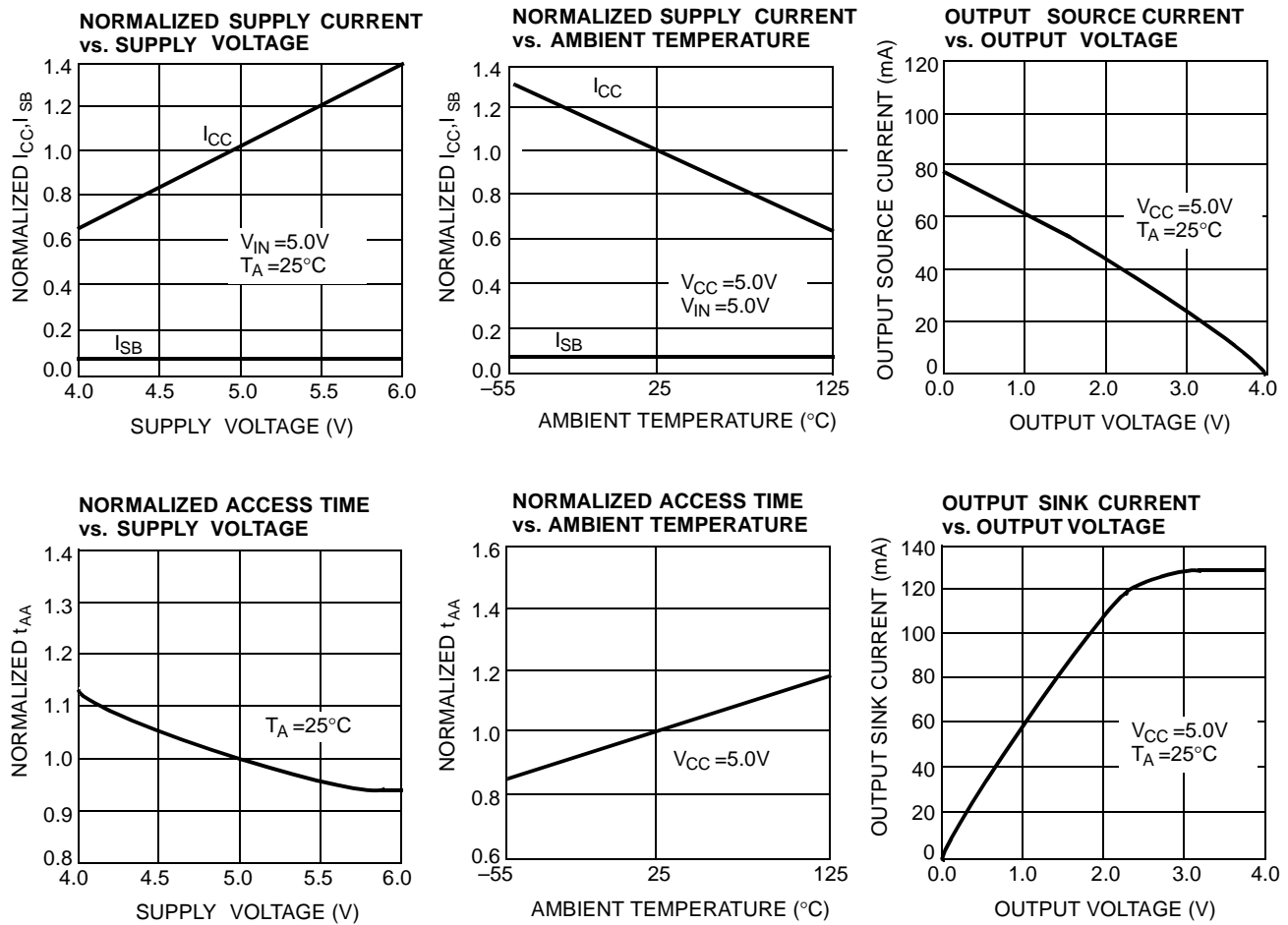
C199-11

**Notes:**

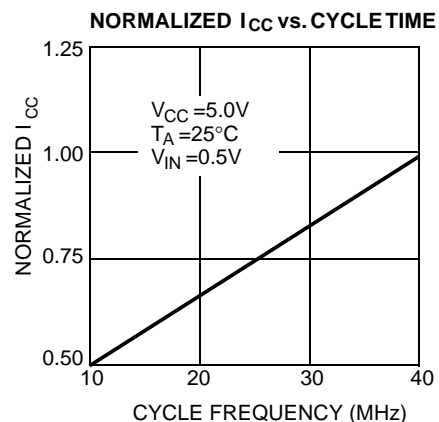
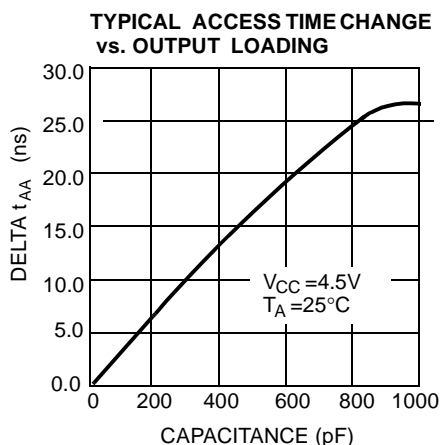
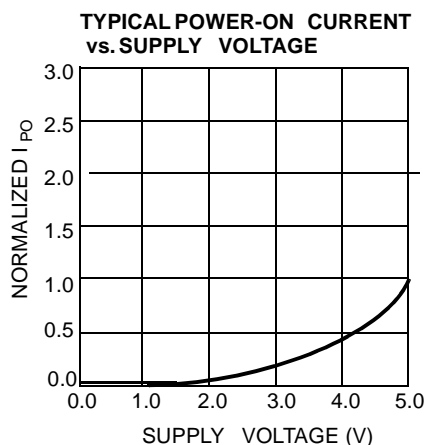
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
15. Data I/O is high impedance if  $OE = V_{IH}$ .
16. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 3 (WE Controlled  $\overline{OE}$  LOW)<sup>[11, 16]</sup>**


C199-12

**Typical DC and AC Characteristics**




**Typical DC and AC Characteristics (continued)**

**Truth Table**

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C199-8VC	V21	28-Lead Molded SOJ	Commercial
	CY7C199-8ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-8VC	V21	28-Lead Molded SOJ	
	CY7C199L-8ZC	Z28	28-Lead Thin Small Outline Package	
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial
	CY7C199-10ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-10VC	V21	28-Lead Molded SOJ	
	CY7C199L-10ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-10VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-10ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-10VI	V21	28-Lead Molded SOJ	
	CY7C199L-10ZI	Z28	28-Lead Thin Small Outline Package	
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-12VC	V21	28-Lead Molded SOJ	
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199L-12VC	V21	28-Lead Molded SOJ	
	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-12VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-12ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-12VI	V21	28-Lead Molded SOJ	
	CY7C199L-12ZI	Z28	28-Lead Thin Small Outline Package	

Shaded area contains advance information. Contact your Cypress sales representative for availability

**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-15VC	V21	28-Lead Molded SOJ	
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199L-15VC	V21	28-Lead Molded SOJ	
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-15VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-15ZI	Z28	28-Lead Thin Small Outline Package	Military
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-20VC	V21	28-Lead Molded SOJ	
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199L-20VC	V21	28-Lead Molded SOJ	
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-20VI	V21	28-Lead Molded SOJ	Industrial
	CY7C199-20ZI	Z28	28-Lead Thin Small Outline Package	Military
	CY7C199-20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199L-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-25SC	S21	28-Lead Molded SOIC	
	CY7C199-25VC	V21	28-Lead Molded SOJ	
	CY7C199-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-25ZI	Z28	28-Lead Thin Small Outline Package	Industrial
	CY7C199-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199-35SC	S21	28-Lead Molded SOIC	
	CY7C199-35VC	V21	28-Lead Molded SOJ	
	CY7C199-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains advance information. Contact your Cypress sales representative for availability

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**
**DC Characteristics**

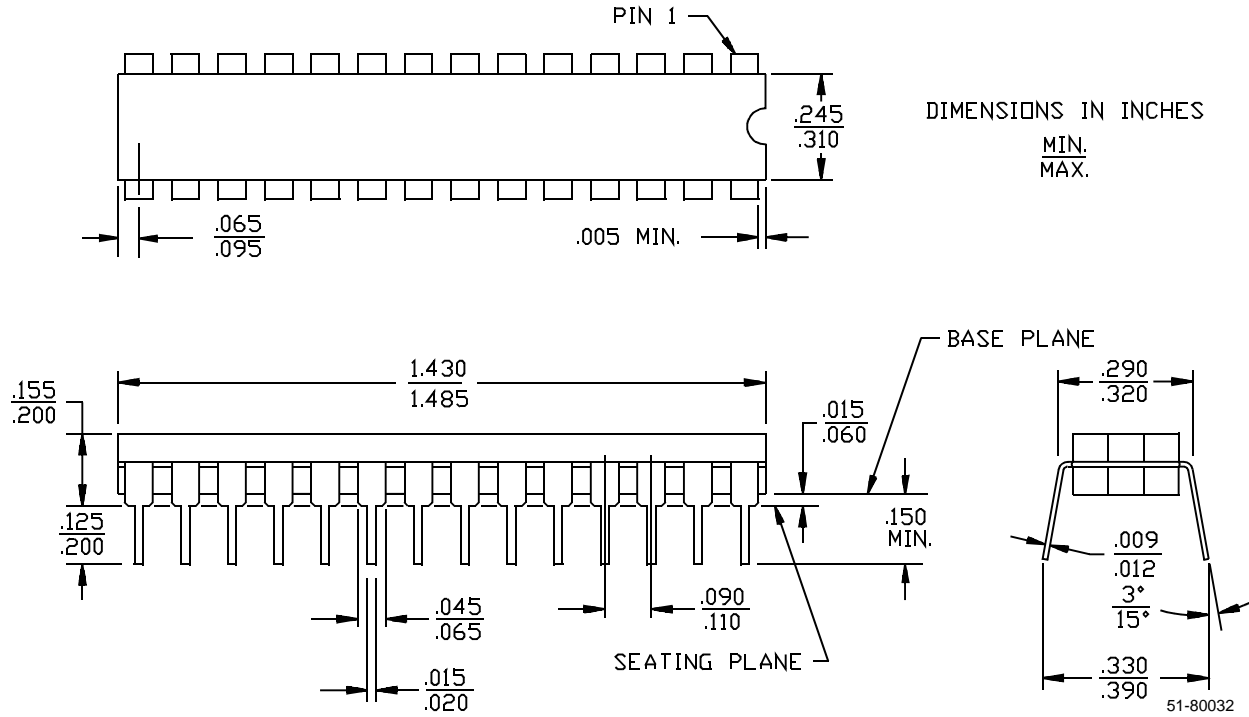
Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL Max.}$	1, 2, 3
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB2}$	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{OHA}$	7, 8, 9, 10, 11
$t_{ACE}$	7, 8, 9, 10, 11
$t_{DOE}$	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11

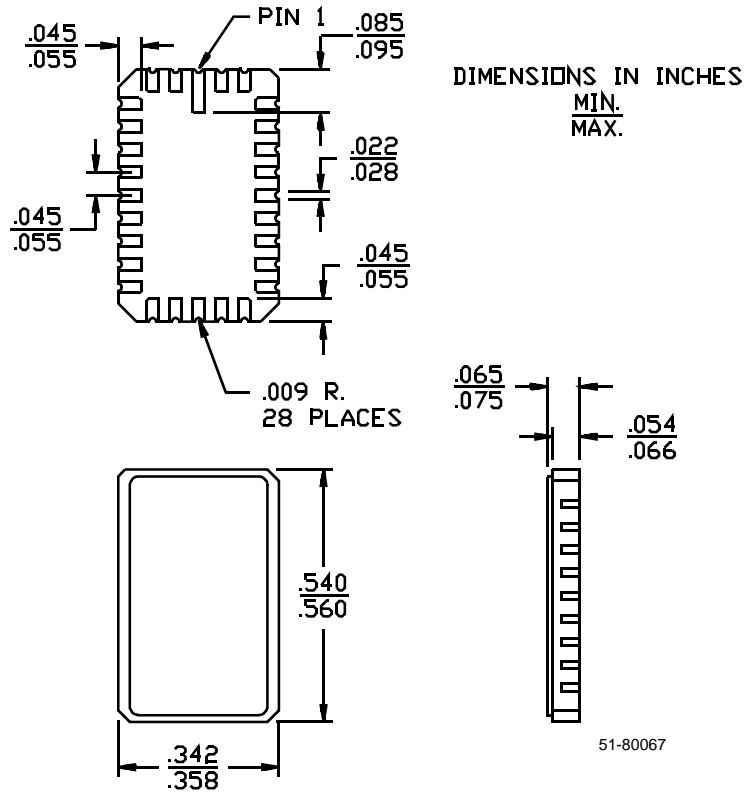
Package Diagrams

**28-Lead (300-Mil) CerDIP D22**  
MIL-STD-1835 D-15 Config. A

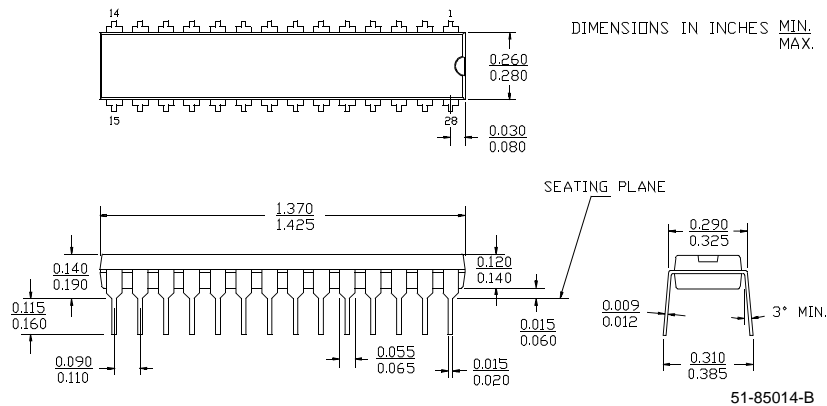


Package Diagrams (continued)

**28-Pin Rectangular Leadless Chip Carrier L54**  
MIL-STD-183C-11A

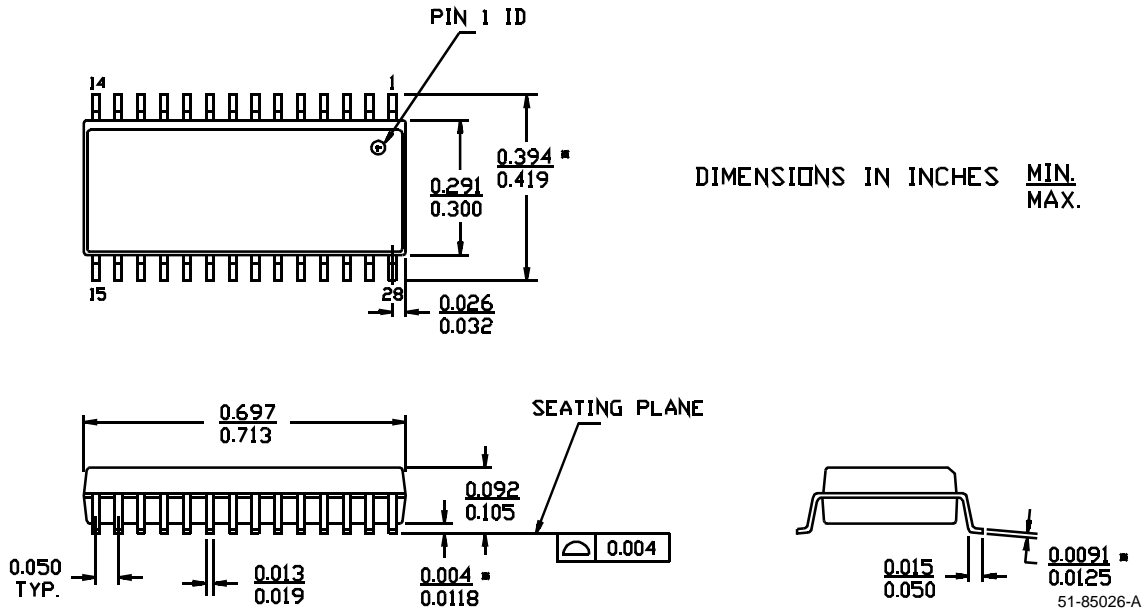


**28-Lead (300-Mil) Molded DIP P21**

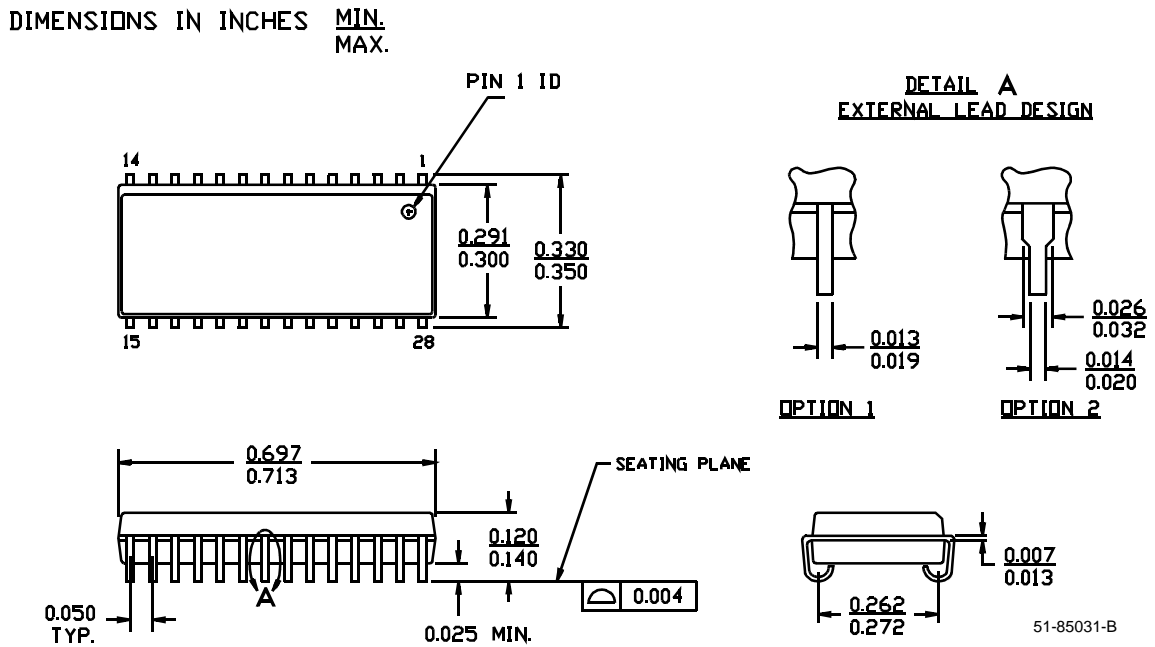


Package Diagrams (continued)

28-Lead (300-Mil) Molded SOIC S21

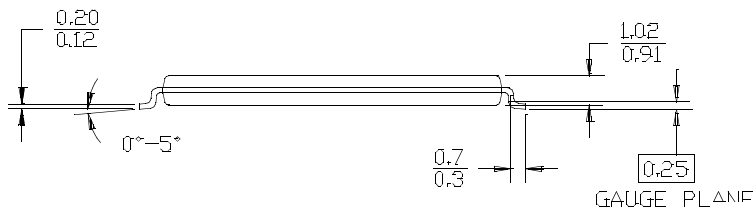
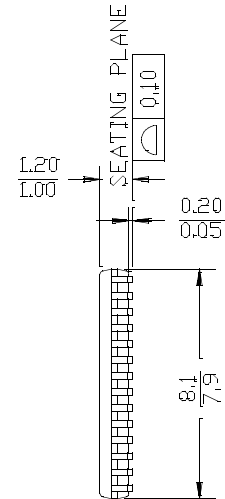
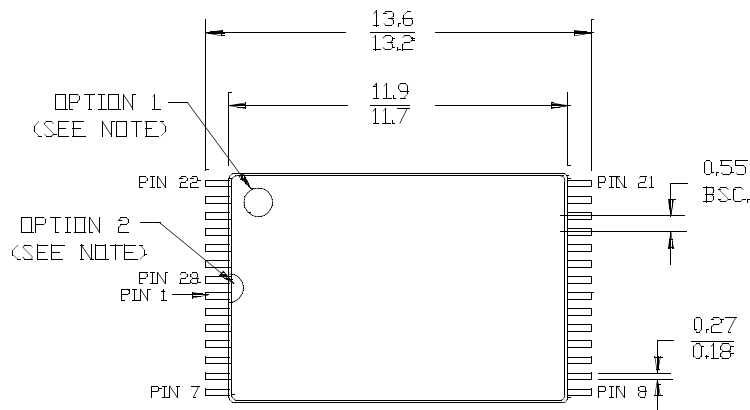


28-Lead (300-Mil) Molded SOJ V21



**Package Diagrams (continued)**
**28-Lead Thin Small Outline Package Z28**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



DIMENSION IN MM  
MAX.  
MIN.

51-85071-F

<b>Document Title: CY7C199 32K x 8 Static RAM</b> <b>Document Number: 38-05160</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109971	10/28/01	SZV	Change from Spec number: 38-00239 to 38-05160