



PAL® 20 Series

16L8/16R8

16R6/16R4

4.5-ns, Industry-Standard PLDs

Features

- Ultra high speed supports today's and tomorrow's fastest microprocessors
 - $t_{PD} = 4.5 \text{ ns}$
 - $t_S = 2.5 \text{ ns}$
 - $f_{MAX} = 142.9 \text{ MHz}$ (external)
- Popular industry standard architectures
- Power-up RESET
- High reliability
 - Proven Ti-W fuses
 - AC and DC tested at the factory
- Security fuse

Functional Description

Cypress PAL20 Series devices consist of the PAL16L8, PAL16R8, PAL16R6, and PAL16R4. Using BiCMOS process and Ti-W fuses, these devices implement the familiar sum-of-products (AND-OR) logic structure.

The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms while the OR array sums selected terms at the outputs.

The product selector guide details all the different options available. All the regis-

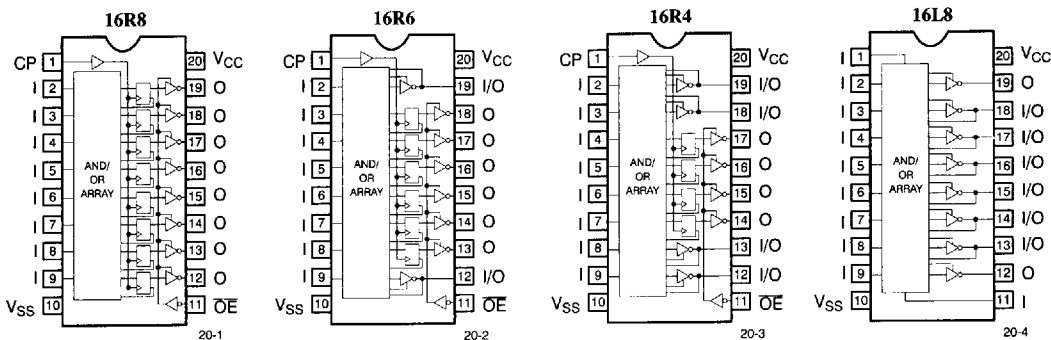
tered devices feature power-up RESET. The register Q output is set to a logic LOW when power is applied to the devices.

A security fuse is provided on all the devices to prevent copying of the device fuse pattern.

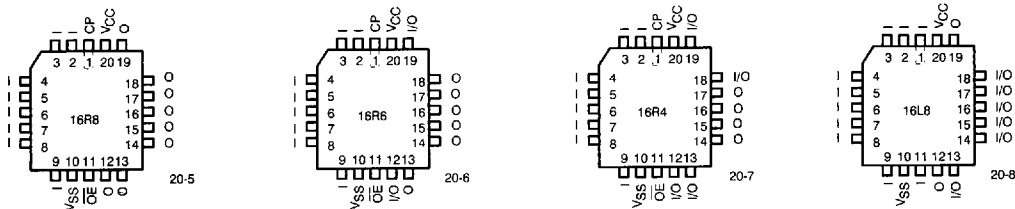
Programming

The PAL20 Series devices can be programmed using the *Impulse* programmer available from Cypress Semiconductor. See third party information in thirdparty tool section for further programmer information.

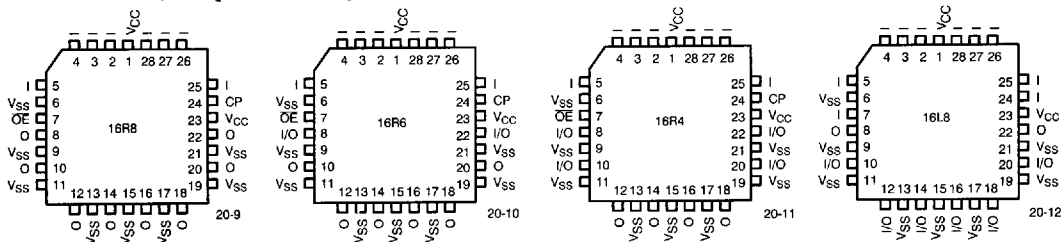
Logic Symbols and DIP Pinouts



20-Pin PLCC/LCC Pinouts



28-Pin PLCC (-4 Speed Bin Only) Pinouts



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Function Selection Guide

| Device | Dedicated Inputs | Outputs | Product Terms/Outputs | Feedback | Enable |
|---------|------------------|--------------------|-----------------------|-------------|----------------|
| PAL16L8 | 10 | 6 comb. 2 comb. | 7 7 | I/O — | prog. prog. |
| PAL16R8 | 8 | 8 reg. | 8 | reg. | pin |
| PAL16R6 | 8 | 6 reg. 2 comb. | 8 7 | reg. I/O | pin prog. |
| PAL16R4 | 8 | 4 reg. 4 comb. | 8 7 | reg. I/O | pin prog. |

Speed Selection Guide (Commercial -4/-5/-7, Military -7/-10)

| Speed Bin | t _{pp} (ns) | t _S (ns) | t _{CO} (ns) | f _{MAX} (MHz) | I _{CC} (mA) |
|-----------|----------------------|---------------------|----------------------|------------------------|----------------------|
| -4 | 4.5 | 2.5 | 4.5 | 142.9 | 180 |
| -5 | 5 | 2.5 | 5 | 133.3 | 180 |
| -7 | 7 | 3.5 | 6 | 105.3 | 180 |
| -10 | 10 | 4.5 | 7 | 87.0 | 180 |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State -0.5V to V_{CC} + 0.5V

DC Input Voltage -1.2V to V_{CC} + 0.5V

DC Input Current

(except during programming) -30 mA to +5 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ±5% |
| Military ^[1] | -55°C to +125°C | 5V ±10% |

DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | Min. | Max. | Unit | |
|-----------------|------------------------------|---|-------------------------|------------|------|------|----|
| | | I _{OH} = -3.2 mA | Commercial | | | | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OH} = -2 mA | Military | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., V _{IN} = V _{IH} or V _{IL} | I _{OL} = 24 mA | Commercial | | 0.5 | V |
| | | | I _{OL} = 12 mA | Military | | | |
| V _{IH} | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for All Inputs ^[2] | | 2.0 | | | V |
| V _{IL} | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for All Inputs ^[2] | | | 0.8 | | V |
| I _{IX} | Input Leakage Current | 0.4V ≤ V _{IN} ≤ 2.7V, V _{CC} = Max. ^[3] | | -250 | 50 | | μA |
| I _I | Maximum Input Current | V _{IN} = 5.5V, V _{CC} = Max. | | | 1 | | mA |
| I _{OZ} | Output Leakage Current | V _{CC} = Max., V _{SS} ≤ V _{OUT} ≤ V _{CC} ^[3] | | -100 | +100 | | μA |
| I _{SC} | Output Short Circuit Current | V _{CC} = Max., V _{OUT} = 0.5V ^[4] | | -30 | -130 | | mA |
| I _{CC} | Power Supply Current | V _{CC} = Max., V _{IN} = GND, Outputs Open | | | 180 | | mA |

Notes:

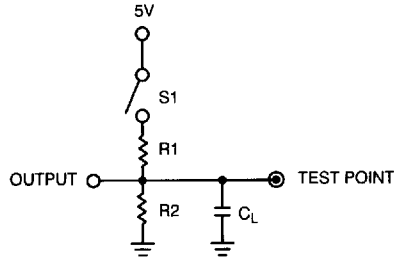
- T_A is the "instant on" case temperature.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- I/O pin leakage is the worse case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.



Capacitance^[5]

| Parameter | Description | | Test Conditions | Typical | Unit |
|------------------|--------------------|---------------------------------|--|---------|------|
| C _{IN} | Input Capacitance | CP, OE | T _A = 25°C, f = 1 MHz, V _{IN} = 0, V _{CC} = 5.0V | 8 | pF |
| | | I ₁ - I ₈ | | 5 | pF |
| C _{OUT} | Output Capacitance | | | 8 | pF |

AC Test Loads and Waveforms



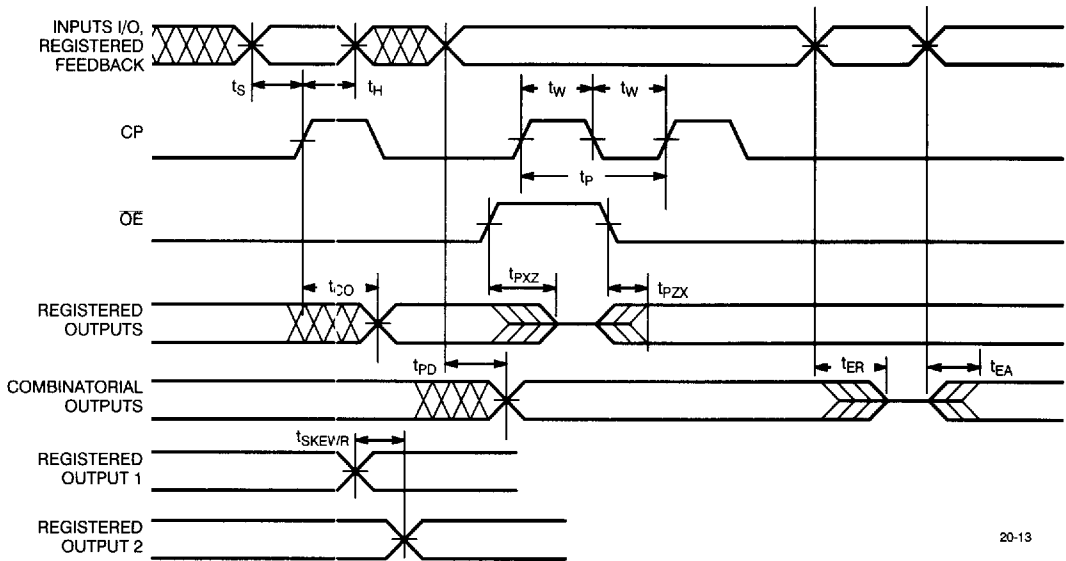
| Specification | S ₁ | C _L | Commercial | | Military | | Measured Output Value |
|------------------------------------|------------------------------|----------------|----------------|----------------|----------------|----------------|--|
| | | | R ₁ | R ₂ | R ₁ | R ₂ | |
| t _{PD} , t _{CO} | Closed | 50 pF | 200Ω | 390Ω | 390Ω | 750Ω | 1.5V |
| t _{PZX} , t _{EA} | Z ↗ H: Open Z ↘ L: Closed | 5 pF | | | | | 1.5V |
| t _{PXZ} , t _{ER} | H ↗ Z: Open L ↗ Z: Closed | | | | | | H ↗ Z: V _{OH} - 0.5V L ↗ Z: V _{OL} + 0.5V |

Switching Characteristics Over the Operating Range^[6]

| Parameter | Description | -4 | | -5 | | -7 | | -10 | | Unit | |
|--------------------|---|---|------|------|-------|------|-------|------|-------|------|-----|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PD} | Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4 | 1 | 4.5 | 1 | 5 | 2 | 7 | 2 | 10 | ns | |
| t _{EA} | Input to Output Enable 16L8, 16R6, 16R4 | 2 | 6.5 | 2 | 6.5 | 2 | 7 | 2 | 10 | ns | |
| t _{ER} | Input to Output Disable Delay 16L8, 16R6, 16R4 | 2 | 5.5 | 2 | 5.5 | 2 | 7 | 2 | 10 | ns | |
| t _{PZX} | Pin 11 to Output Enable 16R8, 16R6, 16R4 | 1 | 6 | 1 | 6 | 2 | 7 | 2 | 10 | ns | |
| t _{PXZ} | Pin 11 to Output Disable 16R8, 16R6, 16R4 | 1 | 5 | 1 | 5 | 2 | 7 | 2 | 10 | ns | |
| t _{CO} | Clock to Output 16R8, 16R6, 16R4 | 1 | 4.5 | 1 | 5 | 2 | 6 | 2 | 7 | ns | |
| t _{SKEWR} | Skew Between Registered Outputs 16R8, 16R6, 16R4 ^[5] | | 0.75 | | 1 | | 1 | | 1 | ns | |
| t _S | Input or Feedback Set-Up Time 16R8, 16R6, 16R4 | 2.5 | | 2.5 | | 3.5 | | 4.5 | | ns | |
| t _H | Hold Time 16R8, 16R6, 16R4 | 0 | | 0 | | 0 | | 0 | | ns | |
| t _p | Clock Period (t _{CO} + t _S) | 7 | | 7.5 | | 9.5 | | 11.5 | | ns | |
| t _w | Clock Width | 3 | | 3 | | 3.5 | | 5 | | ns | |
| f _{MAX} | Maximum Frequency | External Feedback (1/tp) ^[7] | | | 142.9 | | 133.3 | | 105.3 | 87 | MHz |
| | | Internal Feedback ^[5, 8] | | | 175 | | 175 | | 150 | 133 | |

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- See the last page of this specification for Group A subgroup testing information.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
- This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal-only feedback can operate.

Switching Waveforms^[9]


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Note:

9. Input rise and fall time is 2-ns typical.

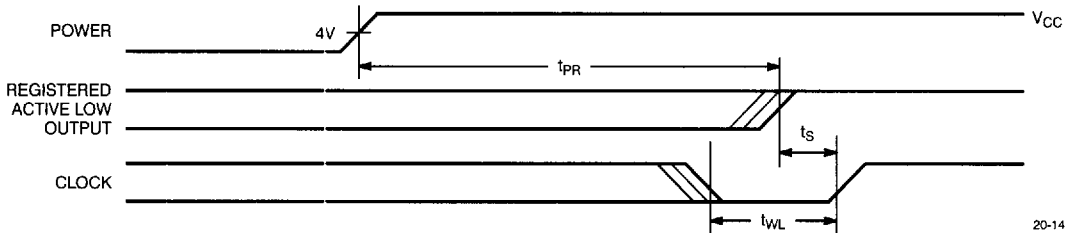
Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways

V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback set-up times are met.

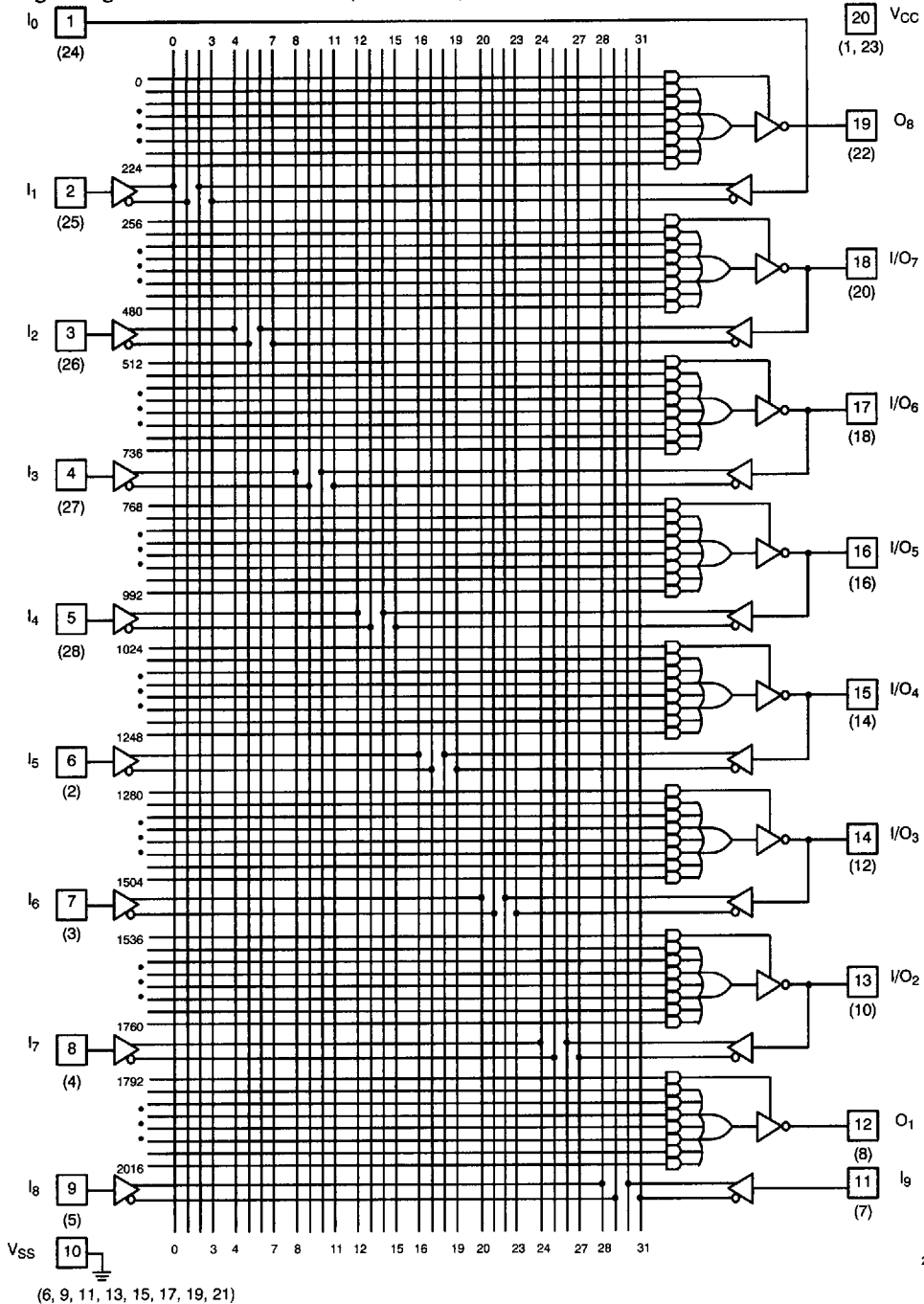
| Parameter Symbol | Parameter Description | Max. | Unit |
|------------------|-------------------------------|-------------------------------|------|
| t_{PR} | Power-Up Reset Time | 1000 | ns |
| t_s | Input or Feedback Set-Up Time | See Switching Characteristics | |
| t_{WL} | Clock Width LOW | | |

Power-Up Reset Waveform


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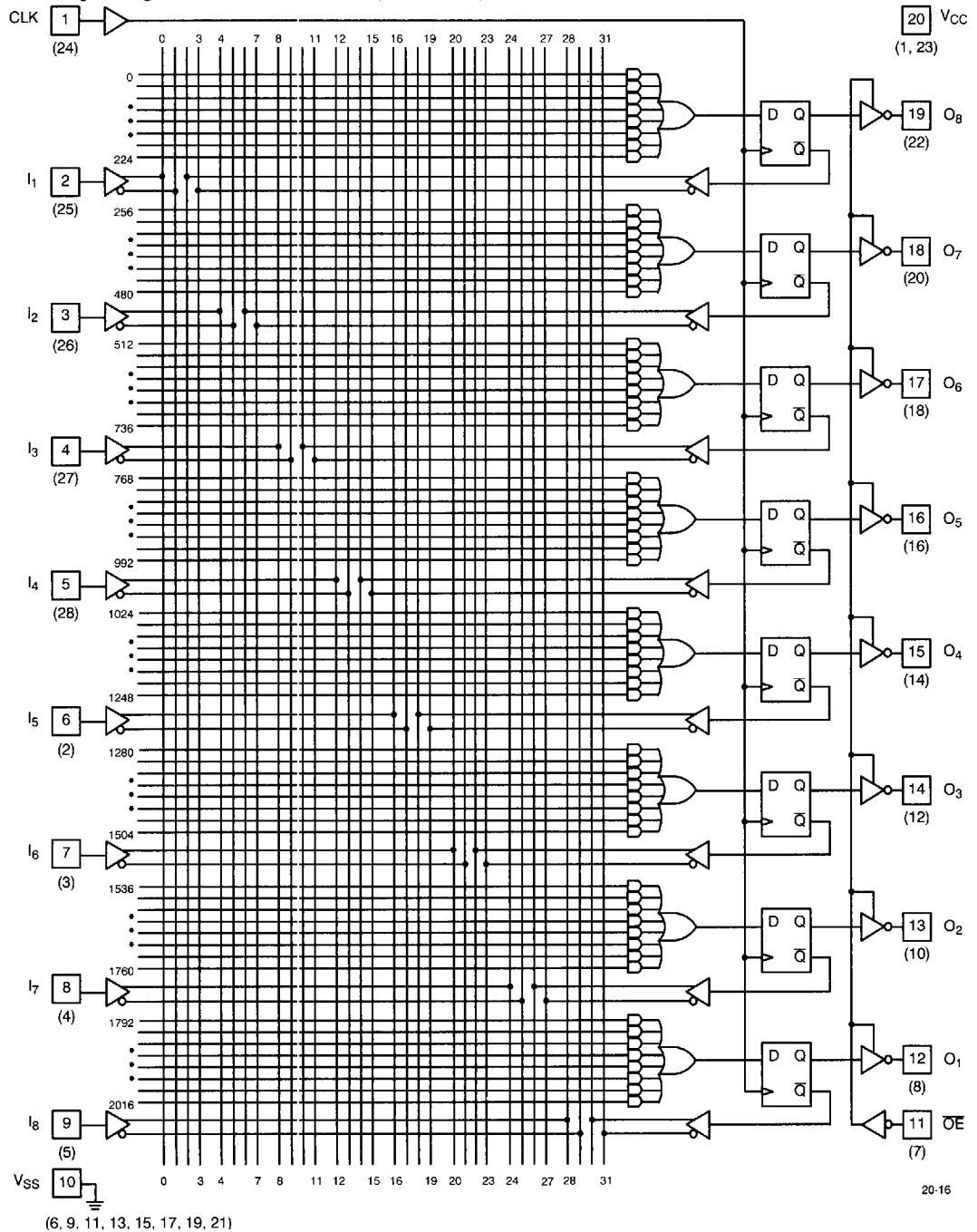


16L8 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



20-15

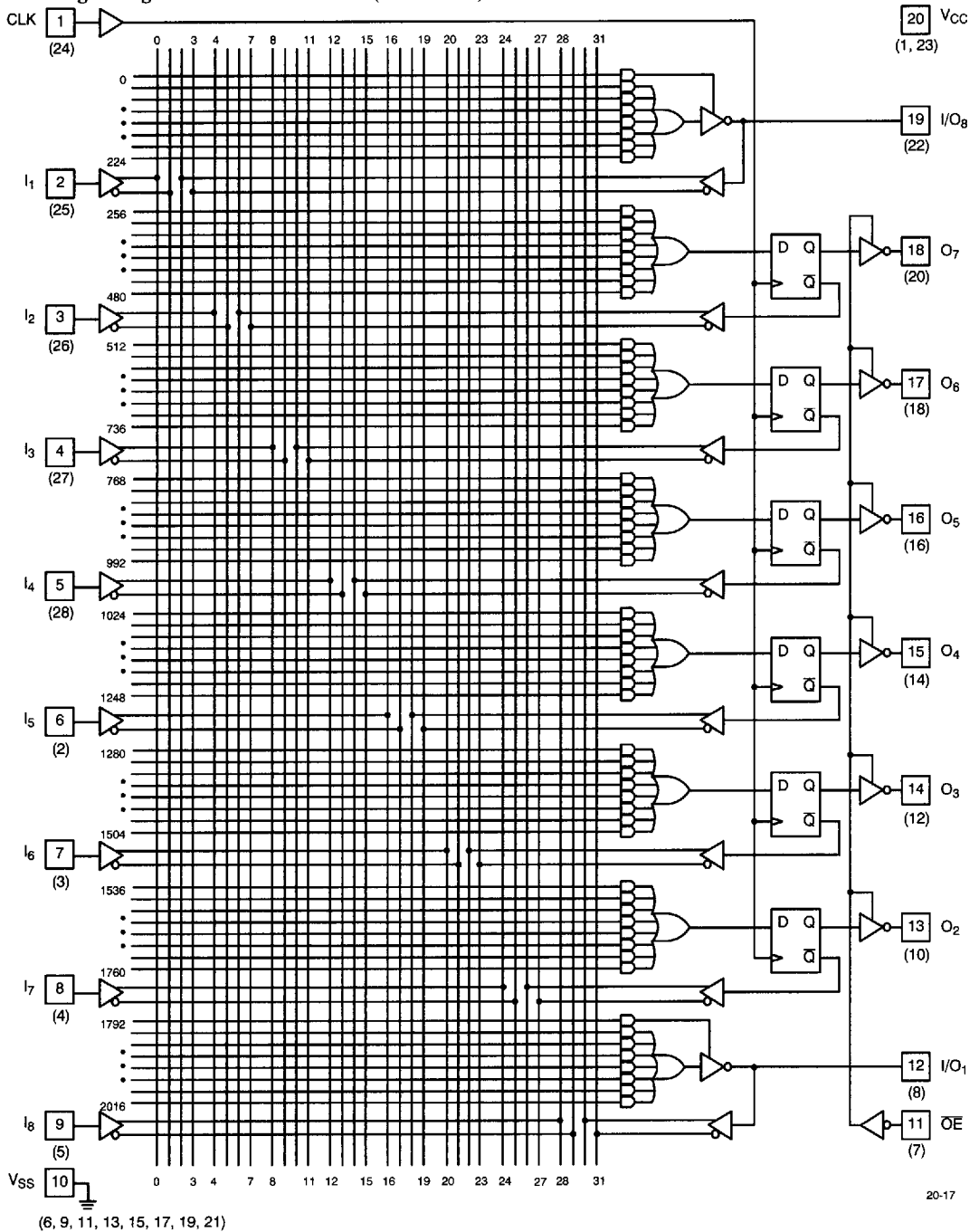
16R8 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



2

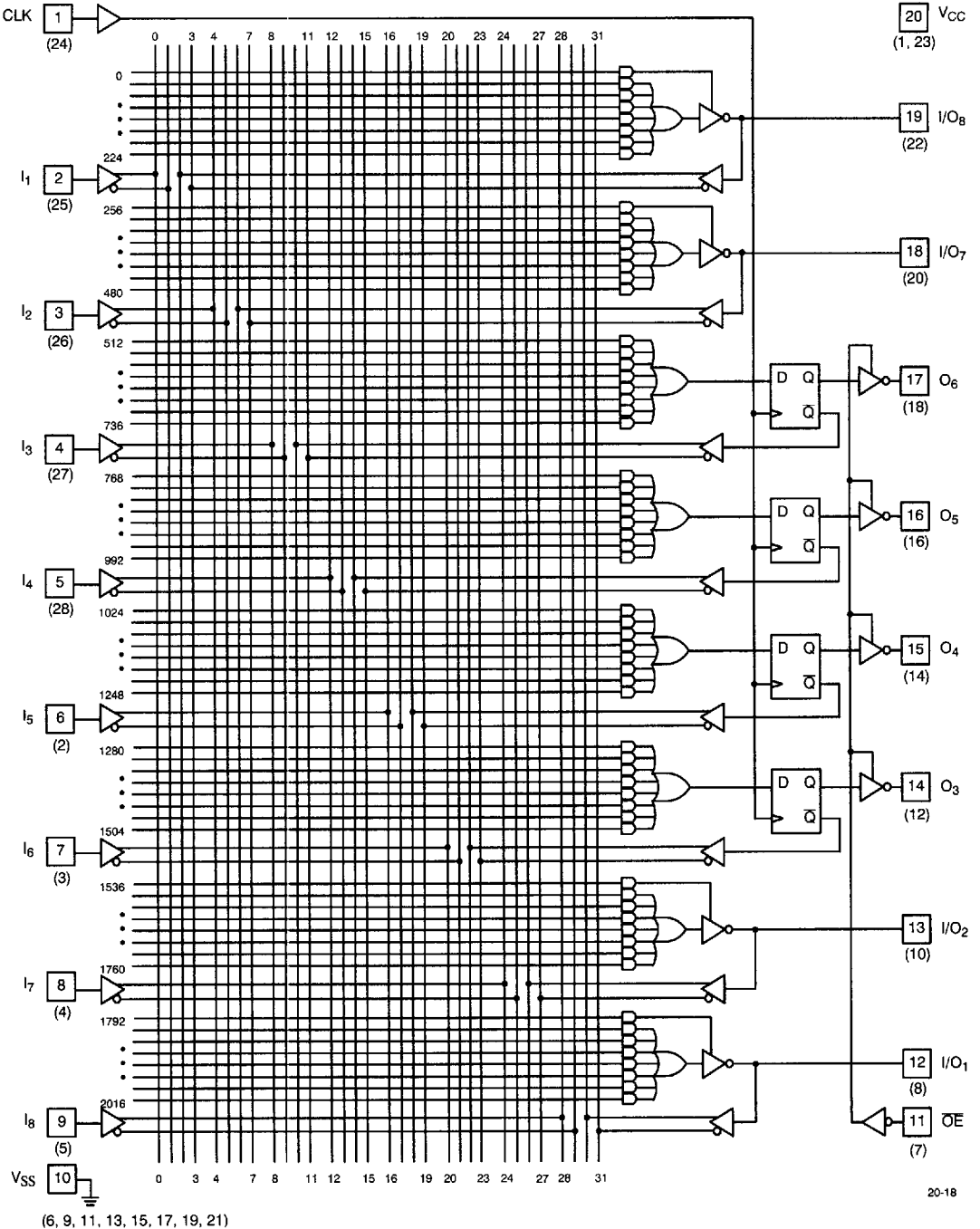


16R6 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



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16R4 Logic Diagram 20-Pin DIP/PLCC/LCC (28-Pin PLCC) Pinouts



2



Ordering Information

| I _{CC} (mA) | t _{PD} (ns) | Ordering Code | Package Name | Package Type | Operating Range | | |
|----------------------|----------------------|---------------|---------------|-------------------------------------|-----------------|-------------------------------------|-------------------------------------|
| 180 | 4.5 | PAL16L8-4JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial | | |
| | | 5 | PAL16L8-5DC | D6 | | 20-Lead (300-Mil) CerDIP | |
| | PAL16L8-5JC | | J61 | 20-Lead Plastic Leaded Chip Carrier | | | |
| | PAL16L8-5PC | | P5 | 20-Lead (300-Mil) Molded DIP | | | |
| | 7 | 7DC | PAL16L8-7DC | D6 | | 20-Lead (300-Mil) CerDIP | |
| | | | PAL16L8-7JC | J61 | | 20-Lead Plastic Leaded Chip Carrier | |
| | | 7PC | PAL16L8-7PC | P5 | | 20-Lead (300-Mil) Molded DIP | |
| | | | 7DMB | PAL16L8-7DMB | | D6 | 20-Lead (300-Mil) CerDIP |
| | | | | PAL16L8-7LMB | | L61 | 20-Pin Square Leadless Chip Carrier |
| | 10 | 10DMB | PAL16L8-10DMB | D6 | | 20-Lead (300-Mil) CerDIP | Military |
| PAL16L8-10LMB | | | L61 | 20-Pin Square Leadless Chip Carrier | | | |

| I _{CC} (mA) | f _{MAX} (MHz) | Ordering Code | Package Name | Package Type | Operating Range | | |
|----------------------|------------------------|---------------|---------------|-------------------------------------|-----------------|-------------------------------------|-------------------------------------|
| 180 | 142.9 | PAL16R8-4JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial | | |
| | | 133.3 | PAL16R8-5DC | D6 | | 20-Lead (300-Mil) CerDIP | |
| | | | PAL16R8-5JC | J61 | | 20-Lead Plastic Leaded Chip Carrier | |
| | | | PAL16R8-5PC | P5 | | 20-Lead (300-Mil) Molded DIP | |
| | 105.3 | 7DC | PAL16R8-7DC | D6 | | 20-Lead (300-Mil) CerDIP | |
| | | | PAL16R8-7JC | J61 | | 20-Lead Plastic Leaded Chip Carrier | |
| | | 7PC | PAL16R8-7PC | P5 | | 20-Lead (300-Mil) Molded DIP | |
| | | | 7DMB | PAL16R8-7DMB | | D6 | 20-Lead (300-Mil) CerDIP |
| | | | | PAL16R8-7LMB | | L61 | 20-Pin Square Leadless Chip Carrier |
| | 87 | 10DMB | PAL16R8-10DMB | D6 | | 20-Lead (300-Mil) CerDIP | Military |
| PAL16R8-10LMB | | | L61 | 20-Pin Square Leadless Chip Carrier | | | |

| I _{CC} (mA) | t _{PD} (ns) | f _{MAX} (MHz) | Ordering Code | Package Name | Package Type | Operating Range | | |
|----------------------|----------------------|------------------------|---------------|--------------|-------------------------------------|-----------------|-------------------------------------|-------------------------------------|
| 180 | 4.5 | 142.9 | PAL16R6-4JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial | | |
| | | | 5 | 133.3 | PAL16R6-5DC | | D6 | 20-Lead (300-Mil) CerDIP |
| | | | | | PAL16R6-5JC | | J61 | 20-Lead Plastic Leaded Chip Carrier |
| | PAL16R6-5PC | P5 | | | 20-Lead (300-Mil) Molded DIP | | | |
| | 7 | 105.3 | 7DC | PAL16R6-7DC | D6 | | 20-Lead (300-Mil) CerDIP | |
| | | | | PAL16R6-7JC | J61 | | 20-Lead Plastic Leaded Chip Carrier | |
| | | | 7PC | PAL16R6-7PC | P5 | | 20-Lead (300-Mil) Molded DIP | |
| | | | | 7DMB | PAL16R6-7DMB | | D6 | 20-Lead (300-Mil) CerDIP |
| | 10 | 87 | 10DMB | | PAL16R6-10DMB | | D6 | 20-Lead (300-Mil) CerDIP |
| | | | | 10LMB | PAL16R6-10LMB | | L61 | 20-Pin Square Leadless Chip Carrier |

Ordering Information (continued)

| I _{CC} (mA) | t _{PD} (ns) | f _{MAX} (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|-------------------------|-------------------------|---------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-----------------|
| 180 | 4.5 | 142.9 | PAL16R4-4JC | J64 | 28-Lead Plastic Leaded Chip Carrier | Commercial |
| | | | PAL16R4-5DC | D6 | 20-Lead (300-Mil) CerDIP | |
| | PAL16R4-5JC | J61 | 20-Lead Plastic Leaded Chip Carrier | | | |
| | PAL16R4-5PC | P5 | 20-Lead (300-Mil) Molded DIP | | | |
| | 7 | 105.5 | PAL16R4-7DC | D6 | 20-Lead (300-Mil) CerDIP | |
| | | | PAL16R4-7JC | J61 | 20-Lead Plastic Leaded Chip Carrier | |
| | | | PAL16R4-7PC | P5 | 20-Lead (300-Mil) Molded DIP | |
| | | | PAL16R4-7DMB | D6 | 20-Lead (300-Mil) CerDIP | Military |
| | PAL16R4-7LMB | L61 | 20-Pin Square Leadless Chip Carrier | | | |
| | 10 | 87 | PAL16R4-10DMB | D6 | 20-Lead (300-Mil) CerDIP | |
| PAL16R4-10LMB | | | L61 | 20-Pin Square Leadless Chip Carrier | | |

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

| Parameters | Subgroups |
|-----------------|-----------|
| V _{OH} | 1, 2, 3 |
| V _{OL} | 1, 2, 3 |
| V _{IH} | 1, 2, 3 |
| V _{IL} | 1, 2, 3 |
| I _{IX} | 1, 2, 3 |
| V _{PP} | 1, 2, 3 |
| I _{CC} | 1, 2, 3 |
| I _{OZ} | 1, 2, 3 |

Switching Characteristics

| Parameters | Subgroups |
|------------------|-----------|
| t _{PD} | 9, 10, 11 |
| t _{PZX} | 9, 10, 11 |
| t _{CO} | 9, 10, 11 |
| t _S | 9, 10, 11 |
| t _H | 9, 10, 11 |

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