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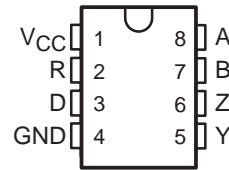


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- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11
- Bus Voltage Range . . . -7 V to 12 V
- Positive- and Negative-Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal-Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)



description

The SN75179B is a differential driver and receiver pair designed for balanced transmission-line applications and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver output provides limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of -7 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The SN75179B is designed to drive current loads of up to 60 mA maximum.

The SN75179B is characterized for operation from 0°C to 70°C.

Function Tables

DRIVER

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$?
$V_{ID} \leq -0.2 \text{ V}$	L
Open	?

H = high level, L = low level, ? = indeterminate



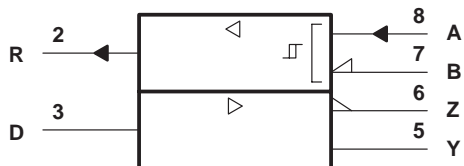
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SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

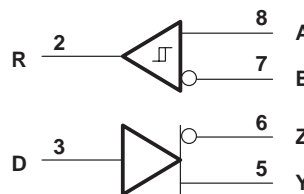
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logic symbol†

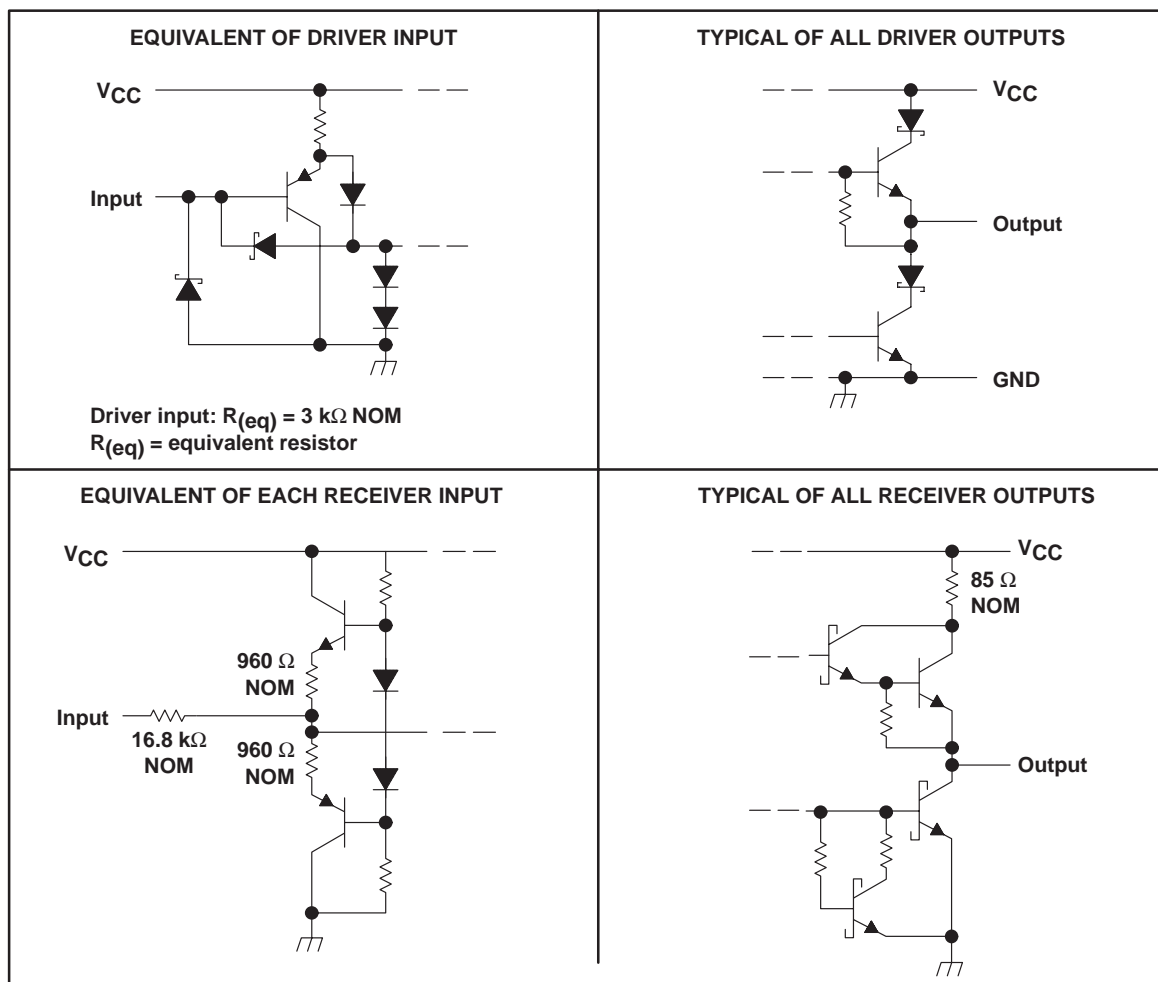


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage range at any bus terminal	–10 V to 15 V
Differential input voltage, V_{ID} (see Note 2)	±25 V
Package thermal impedance, θ_{JA} (see Note 3):	D package
	P package
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		–7‡		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

‡ The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.



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DIFFERENTIAL DRIVER AND RECEIVER PAIR

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	$1/2 V_{OD1}$ or 2^\ddagger			V
	$R_L = 54 \Omega$, See Figure 1	1.5	2.5	5	V
$ V_{OD3} $ Differential output voltage	See Note 4	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of common-mode output voltage§				± 0.2	V
V_{OC} Common-mode output voltage	$R_L = 54 \Omega$ or 100Ω , See Figure 1			$\begin{matrix} 3 \\ -1 \end{matrix}$	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage§				± 0.2	V
I_O Output current	$V_{CC} = 0$, $V_O = -7 \text{ V to } 12 \text{ V}$			± 100	μA
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-200	μA
I_{OS} Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = V_{CC}$ or 12 V			250	
I_{CC} Supply current (total package)	No load		57	70	mA

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The minimum V_{OD2} with $100\text{-}\Omega$ load is either $1/2 V_{OD2}$ or 2 V , whichever is greater.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input changes from a high level to a low level.

NOTE 4: See TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$R_L = 54 \Omega$, See Figure 3		15	22	ns
$t_{t(OD)}$ Differential output transition time			20	30	ns

Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		V_t (Test Termination Measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - \bar{V}_{os} $	$ V_{os} - \bar{V}_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}



RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7\text{ V}$, $I_O = -0.4\text{ mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5\text{ V}$, $I_O = 8\text{ mA}$	-0.2‡			V
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_{OH} High-level output voltage	$V_{ID} = 200\text{ mV}$, $I_{OH} = -400\text{ }\mu\text{A}$, See Figure 2		2.7		V
V_{OL} Low-level output voltage	$V_{ID} = -200\text{ mV}$, $I_{OL} = 8\text{ mA}$, See Figure 2			0.45	V
I_I Line input current	Other input at 0 V, See Note 5			1	mA
				-0.8	
r_i Input resistance			12		k Ω
I_{OS} Short-circuit output current		-15		-85	mA
I_{CC} Supply current (total package)	No load		57	70	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: Refer to TIA/EIA-422-B for exact conditions.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V}$ to 1.5 V , $C_L = 15\text{ pF}$, See Figure 4		19	35	ns
t_{PHL} Propagation delay time, high- to low-level output			30	40	ns

PARAMETER MEASUREMENT INFORMATION

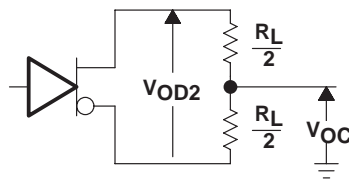


Figure 1. Driver V_{DD} and V_{OC}

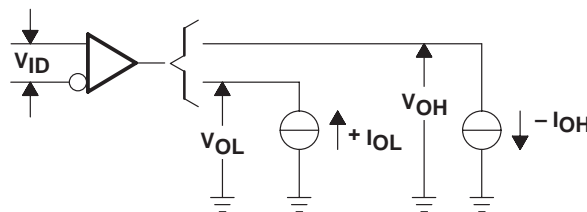
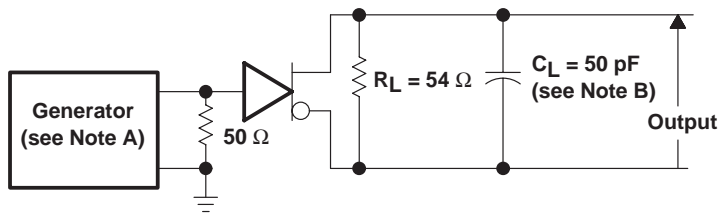


Figure 2. Receiver V_{OH} and V_{OL}

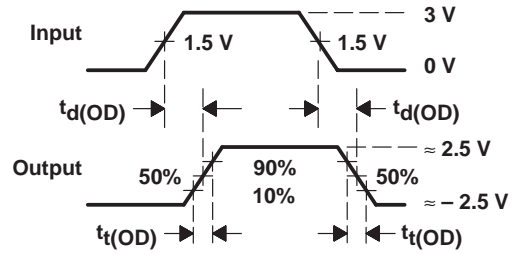
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PARAMETER MEASUREMENT INFORMATION (CONTINUED)



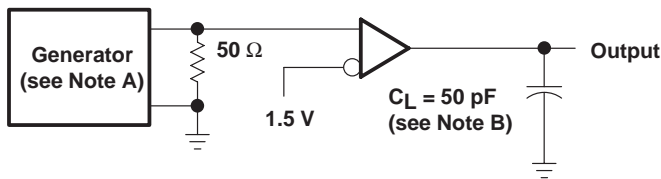
TEST CIRCUIT



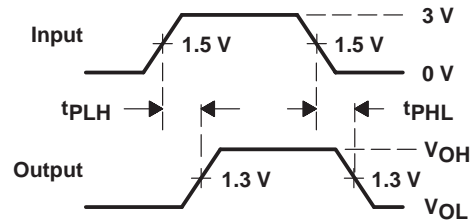
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

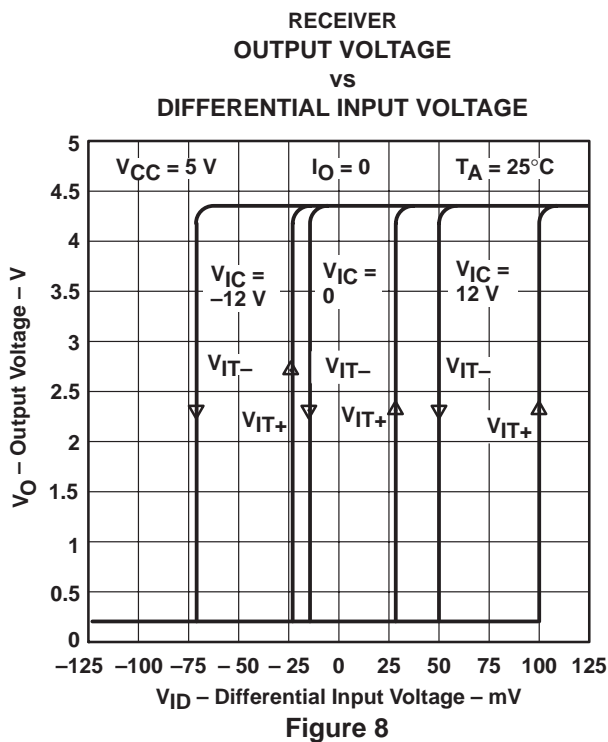
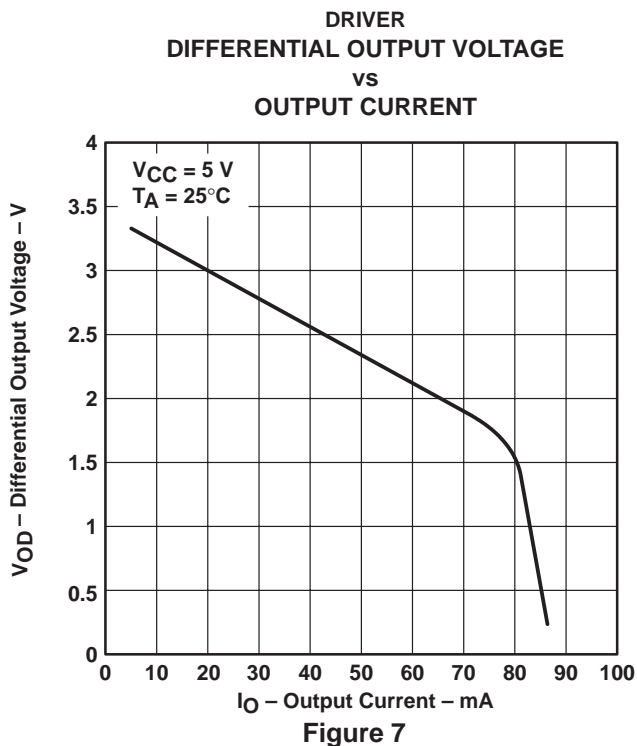
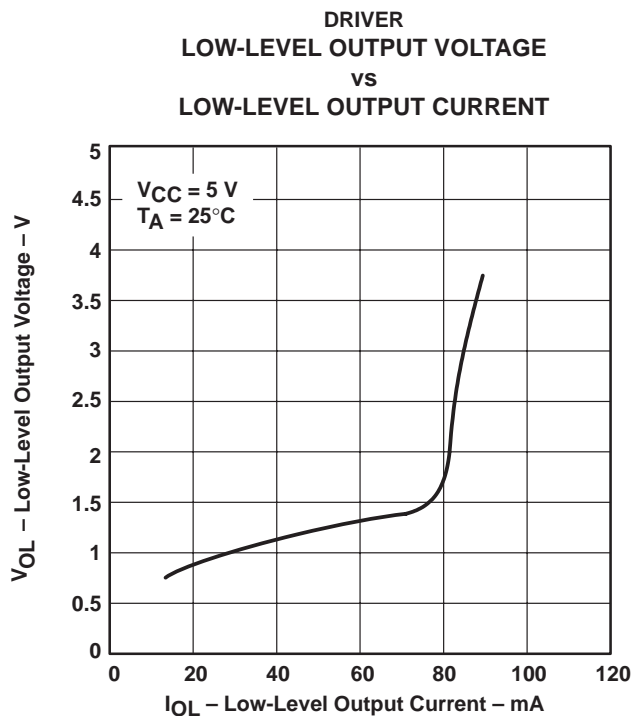
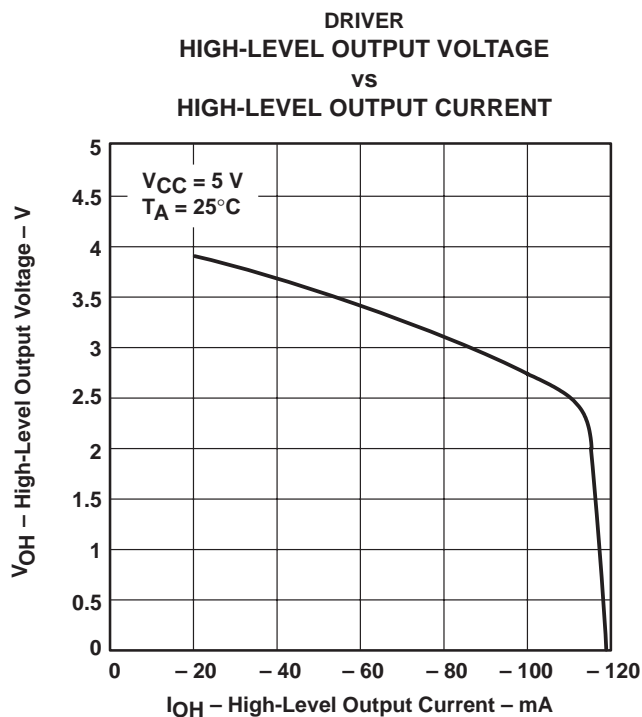


VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

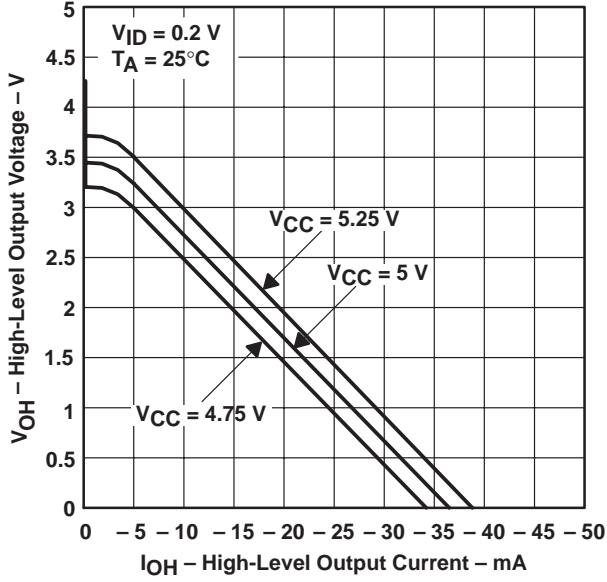


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

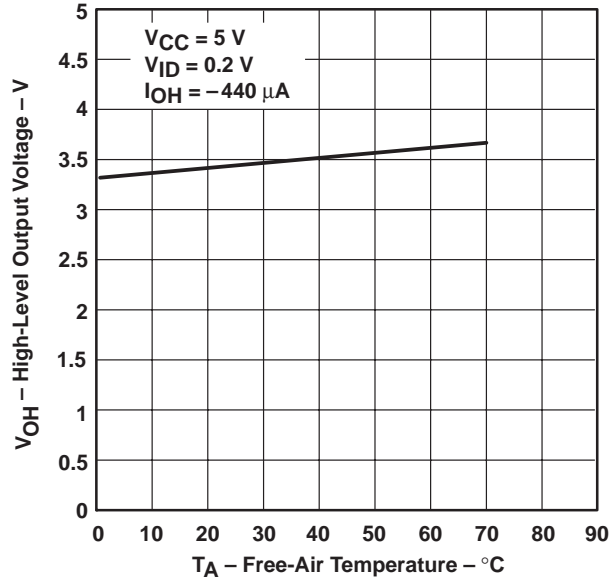


Figure 10

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

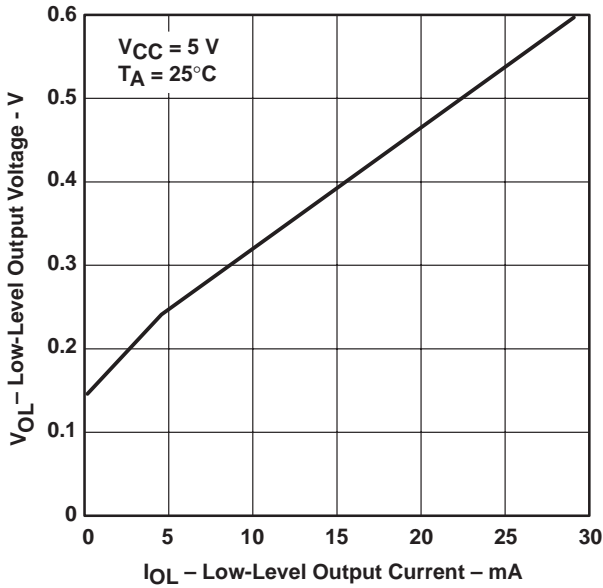


Figure 11

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

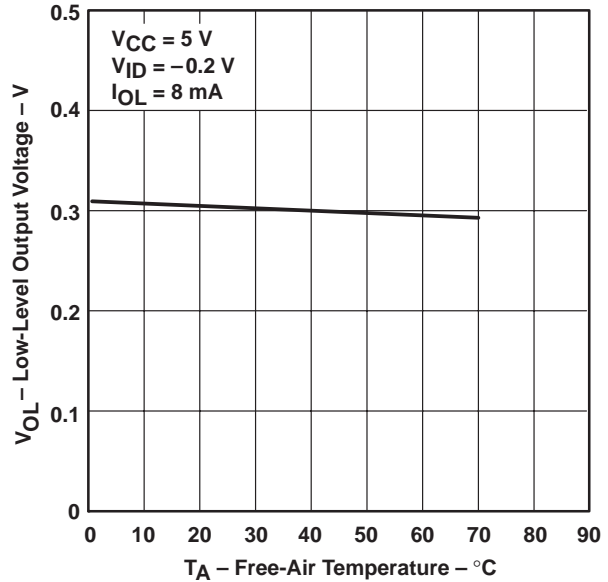


Figure 12

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