

Distributed by:



www.Jameco.com ♦ 1-800-831-4242

The content and copyrights of the attached material are the property of its owner.

Jameco Part Number 287064



April 1988
Revised June 2003

74F86 2-Input Exclusive-OR Gate

74F86 2-Input Exclusive-OR Gate

General Description

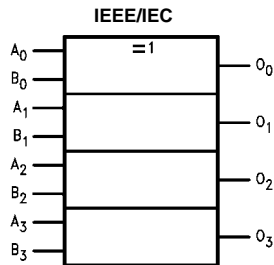
This device contains four independent gates, each of which performs the logic exclusive-OR function.

Ordering Code:

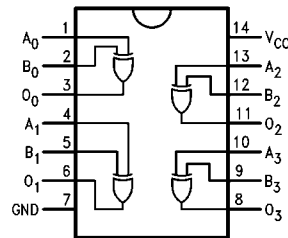
Order Number	Package Number	Package Description
74F86SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F86SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F86PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_n, B_n	Inputs	1.0/1.0	20 μ A/-0.6 mA
O_n	Outputs	50/33.3	-1 mA/20 mA

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

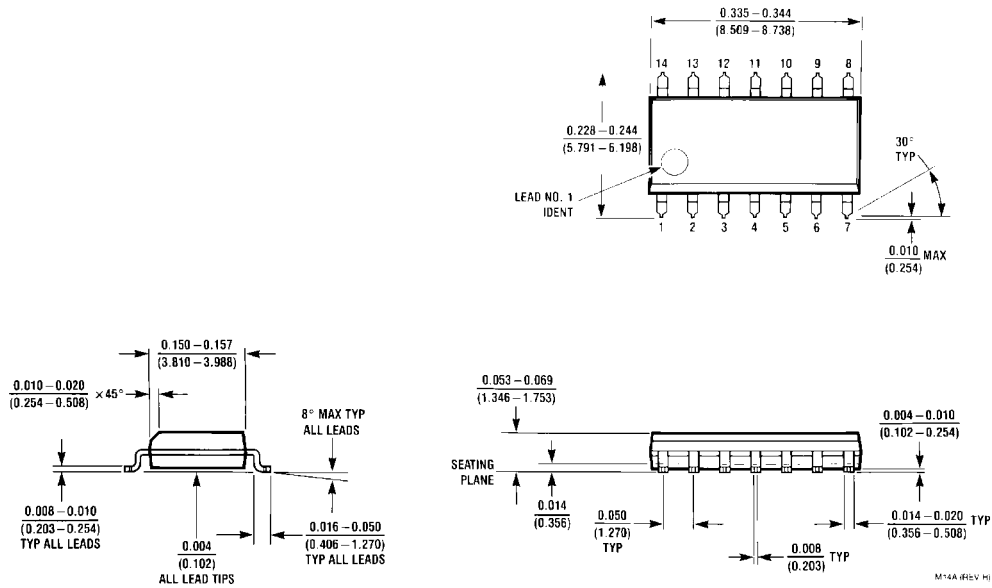
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5		Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All other pins grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All other pins grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		12	18	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		18	28	mA	Max	V _O = LOW

AC Electrical Characteristics

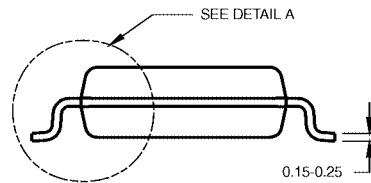
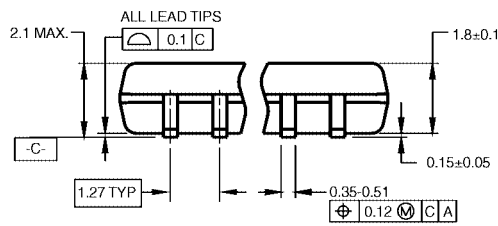
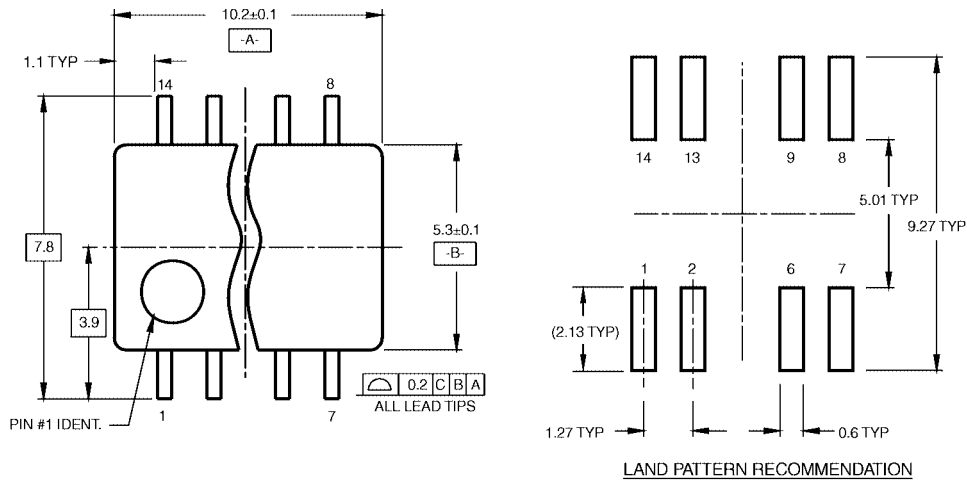
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to O _n (Other Input LOW)	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	ns
t _{PLH} t _{PHL}	Propagation Delay A _n , B _n to O _n (Other Input HIGH)	3.0 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

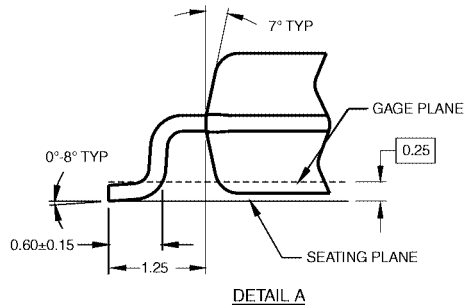
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

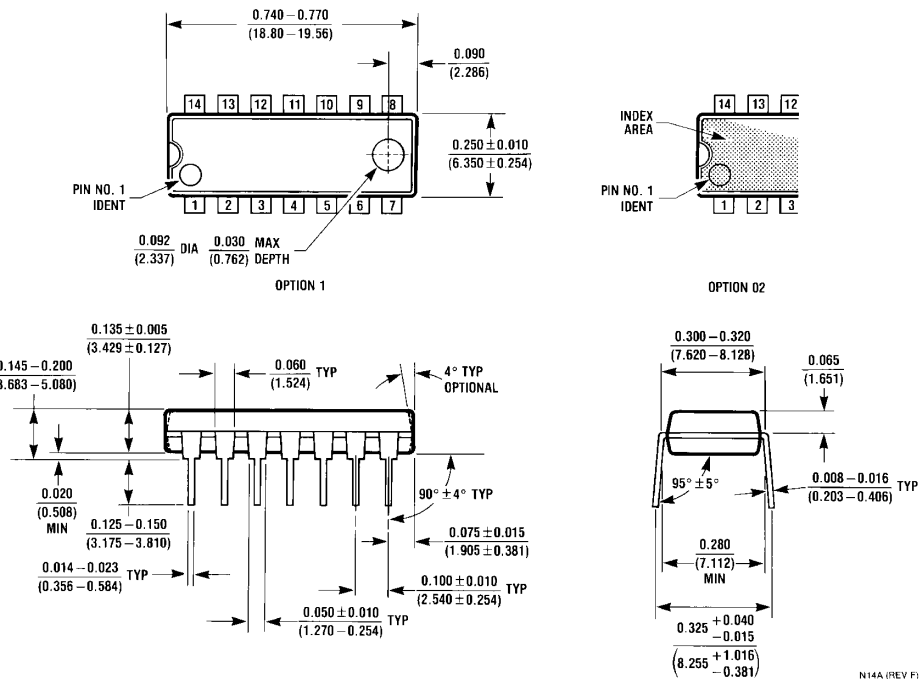
- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com