Jameco Part Number 312514

# PIC12F683

## PIC12F683 Rev. A Silicon/Data Sheet Errata

The PIC12F683 parts you have received conform functionally to the Device Data Sheet (DS41211**B**), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the PIC12F683 silicon.

### 1. Module: Resets (when WDT times out)

If the OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

**Work around**

If a CLRWDT instruction is issued before the WDT times out and before the OPTION register is modified, this problem is eliminated.

**Date Codes that pertain to this issue:**

All engineering and production devices.

## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41211**B**), the following clarifications and corrections should be noted.

### 1. Module: CCP (CCP1CON register)

In Register 11-1, “CCP1CON – Capture/Compare/ PWM Register” the CCP1M<1> functions as an output inversion bit when using the PWM mode. The last line under CCP1M<3:0> should read as shown in Register 11-1 below.

**REGISTER 11-1: CCP1CON – CAPTURE/COMPARE/PWM REGISTER (ADDRESS: 15h)**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 |
| bit 7 | | | | | | | bit 0 |

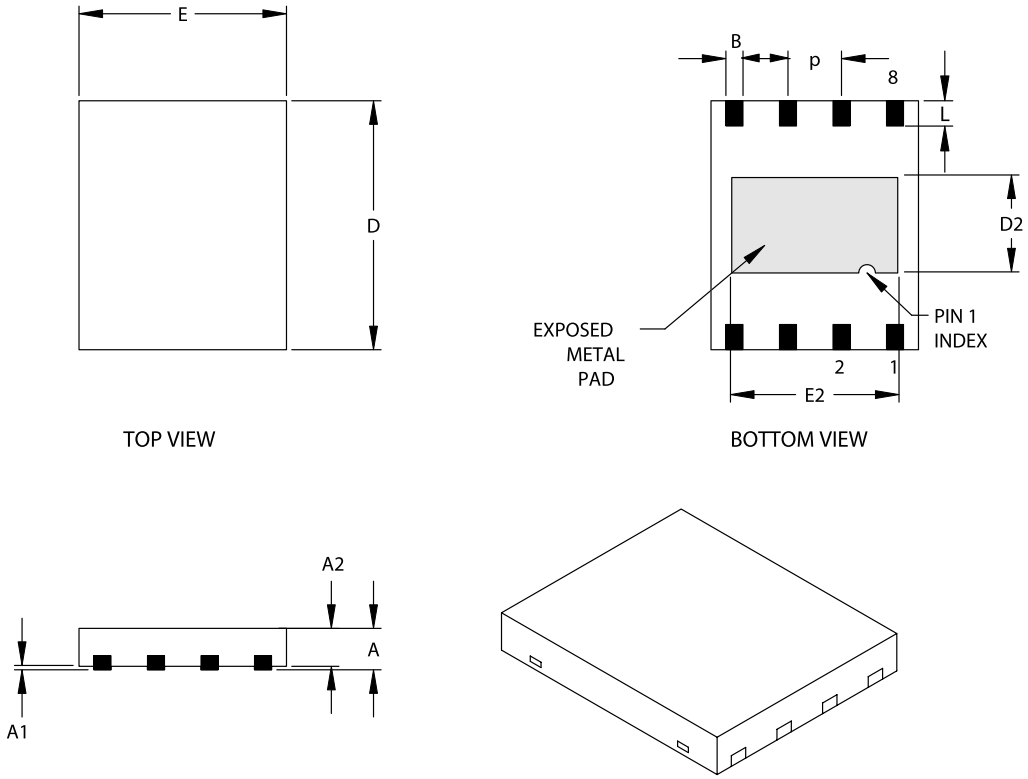
bit 3-0 **CCP1M<3:0>**: CCP1 Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCP1 module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCP1IF bit is set)
1001 = Compare mode, clear output on match (CCP1IF bit is set)
1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 = Compare mode, trigger special event (CCP1IF bit is set, CCP1 pin is unaffected); CCP1 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
**110x = PWM mode active high**
**111x = PWM mode active low**

## 2. Module: Packaging Details

Section 16.2, change “Packaging Details” from the current 8-pin MF packaging (which is no longer used) to the **saw singulated** packaging version, as shown below:

### 8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 8 | | | 8 | |
| Pitch | p | | .050 BSC | | | 1.27 BSC | |
| Overall Height | A | .033 | .035 | .037 | 0.85 | 0.90 | 0.95 |
| Package Thickness | A2 | .031 | .035 | .037 | 0.80 | 0.89 | 0.95 |
| Standoff | A1 | .000 | .0004 | .002 | 0.00 | 0.01 | 0.05 |
| Base Thickness | A3 | .007 | .008 | .009 | 0.17 | 0.20 | 0.23 |
| Overall Length | E | .195 | .197 | .199 | 4.95 | 5.00 | 5.05 |
| Exposed Pad Length | E2 | .152 | .157 | .163 | 3.85 | 4.00 | 4.15 |
| Overall Width | D | .234 | .236 | .238 | 5.95 | 6.00 | 6.05 |
| Exposed Pad Width | D2 | .089 | .091 | .093 | 2.25 | 2.30 | 2.35 |
| Lead Width | B | .014 | .016 | .019 | 0.35 | 0.40 | 0.47 |
| Lead Length | L | .024 | | .026 | 0.60 | | 0.65 |

Notes:

JEDEC equivalent: MO-220

Drawing No. C04-122 Revised 11/3/03

## REVISION HISTORY

Rev A Document (7/2004)

Changes made to CCP1M<1> in the CCP1CON Register. CCP1M<1> changes from 11xx to 111x (inverted mode) and 110x (normal mode).

Rev B Document (8/2004)

Issue 1 – When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Clarification/Corrections to the Data Sheet: Issue 2 – Changed to 8-pin MF **saw singulated** packaging.

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