PIC16F87/88 Rev. B1 Silicon/Data Sheet Errata

The PIC16F87/88 Rev. B1 parts you have received conform functionally to the Device Data Sheet (DS30487**B**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16F87/88 silicon.

The following silicon errata apply only to PIC16F87/88 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F87	00 0111 001	00101
PIC16F88	00 0111 011	00101

1. Module: Internal RC Oscillator

A high Sleep current will exist when the following condition is met and procedures are followed:

CONDITION: FOSC<2:0> (Configuration Word Register 1) bits are configured for any oscillator selection other than the internal RC oscillator.

PROCEDURE:

1. Clock switch occurs anywhere in the application code where the internal RC oscillator is selected via the SCS bits ('10').
2. Sleep mode is entered while the SCS bits are configured for the internal RC oscillator ('10').

Work around

Before Sleep mode is entered, configure or clear the SCS bits ('00') to switch back to the primary clock source that is defined by FOSC<2:0> (Configuration Word Register 1).

2. Module: Internal RC Oscillator IOFS bit

The device data sheet states when an INTOSC frequency is selected (125, 250, 500 kHz, 1, 2, 4, 8 MHz), the frequency will be stable when the IOFS bit becomes set (IOFS = 1) at 4 ms. The following applies for applications relying on time dependent code.

Under the following conditions, any of the INTOSC frequencies may not be stable when IOFS becomes set (IOFS = 1). Devices may vary from one to the next and may take as long as 60 ms to become stable.

1. Wake from Sleep, internal RC oscillator is selected via the SCS bits or Configuration Word 1 and the IRCF bits are configured for an INTOSC frequency.
2. POR is executed, internal RC oscillator is selected via the SCS bits or Configuration Word 1 and the IRCF bits are configured for an INTOSC frequency.
3. The INTRC (31.25 kHz) is clocking the device and a switch to an INTOSC frequency is executed via modification of the IRCF bits.
4. An alternative oscillator selection is clocking the device (i.e., HS mode) and a clock switch to the internal RC oscillator is executed via the SCS bits with the IRCF bits configured for an INTOSC frequency.

Work around

Implement the following software delay shown in Example 1 after an INTOSC frequency has been enabled and before any frequency dependent application code is executed. This routine will delay application execution approximately 2K-150K TCY (instruction cycles are dependent upon the INTOSC frequency) to ensure a stable INTOSC frequency.

Date Codes that pertain to this issue:

All date codes.

EXAMPLE 1: DELAY ROUTINE

```
DlyVarH     equ     <define address based on application requirements>
DlyVarL     equ     <define address based on application requirements>

;Load the delay variable DlyVarH with the following value for the selected frequency:
    ;125kHz 0x0300
    ;250kHz 0x0600
    ;500kHz 0x0C00
    ;1MHz   0x1900
    ;2MHz   0x3100
    ;4MHz   0x6200
    ;8MHz   0xC300
delay                           ;insure the correct data memory bank is selected
                                ; for access of data variables
    CLRF    DlyVarL             ;initialize low delay variable
    MOVLW   0x62                ;initialize high delay variable
    MOVWF   DlyVarH

dly_loop
    DECFSZ  DlyVarL,f           ;decrement low variable
    GOTO    dly_loop
    DECFSZ  DlyVarH,f           ;decrement high variable
    GOTO    dly_loop
RETURN                          ;delay done
```

3. Module: PORTB Pull-ups

When RBPU = 0 (OPTION register), the PORTB weak pull-ups will not be disabled by the input functions of the SSP and/or CCP (Capture mode) module as indicated by the RB1:RB5 I/O block diagrams in **Section 5.0 "I/O Ports"**.

Work around

1. If the SSP and/or CCP (Capture mode) module is enabled, do not enable the PORTB weak pull-ups and use external pull-up resistors.

OR

2. If the SSP and/or CCP (capture mode) module and PORTB pull-ups are enabled, then evaluate the functionality of the SSP (I^2C™/SPI™) or CCP (Capture mode) module to ensure proper operation within your application.

Date Codes that pertain to this issue:

All date codes.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30487**B**), the following clarifications and corrections should be noted.

1. Module: Voltage Reference Specifications

In Table 18-2 “Voltage Reference Specifications”, the Max value for specification #D311, Absolute Accuracy (VRAA Low Range) is incorrectly stated as 1/4 LSb. The correct value is 1/2 LSb.

The following table shows the change in **bold** text.

TABLE 18-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 5.5V, -40°C < TA < +85°C, unless otherwise stated.							
Spec No.	**Characteristics**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D310	Resolution	VRES	VDD/24	—	VDD/32	LSb	
D311	Absolute Accuracy	VRAA	— —	— —	**1/2** 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
D312	Unit Resistor Value (R)*	VRUR	—	2k	—	Ω	
310	Settling Time(1)*	TSET	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from ‘0000’ to ‘1111’.

2. Module: Timer1 Oscillator and In-Circuit Serial Programming™

The following note has been added to clarify operation of the Timer1 oscillator when using In-Circuit Serial Programming or the In-Circuit Debugger.

This note was added to **Section 7.6 “Timer1 Oscillator”** and **Section 15.17 “In-Circuit Serial Programming”**.

Note: The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.

When using the Timer1 oscillator, In-Circuit Serial Programming™ (ICSP™) may not function correctly (high voltage or low voltage), or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD operation, the Timer1 crystal may be damaged.

If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead), or installed after programming. The oscillator loading capacitors may remain in-circuit during ICSP or ICD operation.

3. Module: DC Characteristics

The maximum 2V, 4 MHz RC Oscillator specifications listed in **Section 18.2 "DC Characteristics"** of the device data sheet are incorrectly stated.

The following table shows the current test limits (modified values are shown in **bold**).

18.2 DC Characteristics: Power-down and Supply Current PIC16F87/88 (Industrial) PIC16LF87/88 (Industrial)

PIC16LF87/88 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	PIC16LF87/88	270	**335**	µA	-40°C	VDD = 2.0V	FOSC = 4 MHz (RC Oscillator)(3)
		280	**330**	µA	+25°C		
		285	**330**	µA	+85°C		
	PIC16LF87/88	460	610	µA	-40°C	VDD = 3.0V	
		450	600	µA	+25°C		
		450	600	µA	+85°C		
	All devices	900	1060	µA	-40°C	VDD = 5.0V	
		890	1050	µA	+25°C		
		890	1050	µA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

REVISION HISTORY

Rev A Document (9/2003)
First revision of this document. Data Sheet Clarification issue 1 (Voltage Reference Specifications).

Rev B Document (2/2004)
Added Data Sheet Clarification issue 2 (Timer1 Oscillator and In-Circuit Serial Programming).

Rev C Document (4/2004)
Added silicon issue 1 (Internal RC Oscillator).

Rev D Document (6/2004)
Updated silicon issue 1 (Internal RC Oscillator) and added Data Sheet Clarification issue 3 (DC Characteristics).

Rev E Document (9/2004)
Added silicon issue 2 (Internal RC Oscillator IOFS bit) and 3 (PORTB Pull-ups).

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