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Jameco Part Number 32803NSC

## TP5089 DTMF (TOUCH-TONE) Generator

### General Description

The TP5089 is a low threshold voltage, field-implemented, metal gate CMOS integrated circuit. It interfaces directly to a standard telephone keypad and generates all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A  $\overline{\text{MUTE}} \text{ OUT}$  logic signal, which changes state when any key is depressed, is also provided.

### Features

- 3.5V–10V operation when generating tones
- 2V operation of keyscan and  $\overline{\text{MUTE}}$  logic
- Static sensing of key closures or logic inputs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Output amplitudes proportional to supply voltage
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$  pin

### Block Diagram

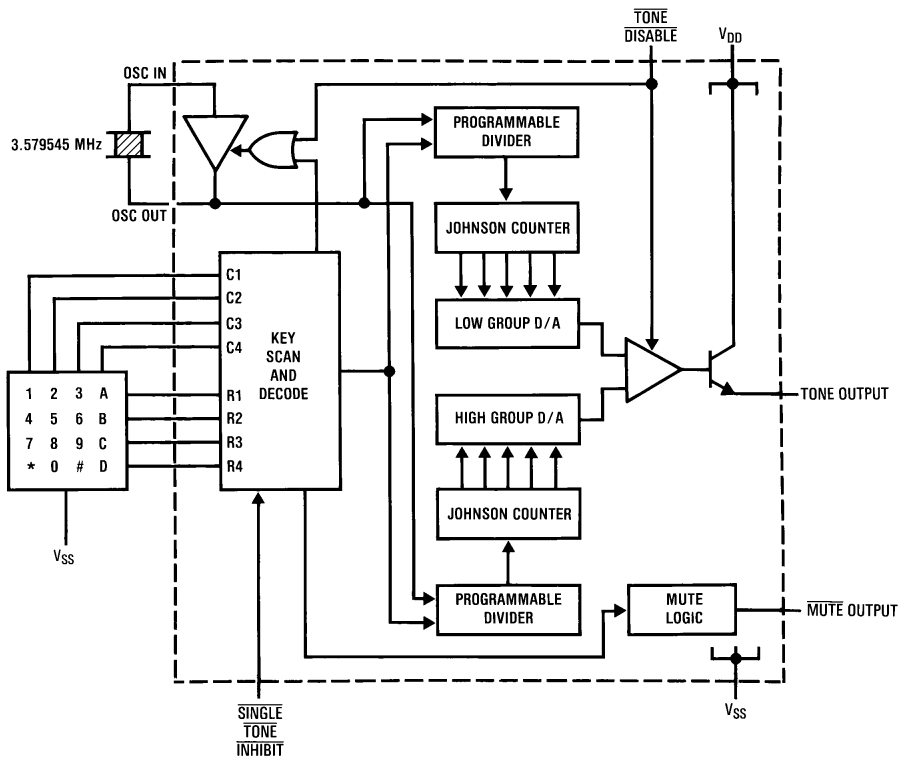


FIGURE 1

TL/H/5057-1

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{DD} - V_{SS}$ ) 15V

Maximum Voltage at Any Pin  $V_{DD} + 0.3V$  to  $V_{SS} - 0.3V$

Operating Temperature  $-30^{\circ}C$  to  $+60^{\circ}C$   
 Storage Temperature  $-55^{\circ}C$  to  $+150^{\circ}C$   
 Maximum Power Dissipation 500 mW

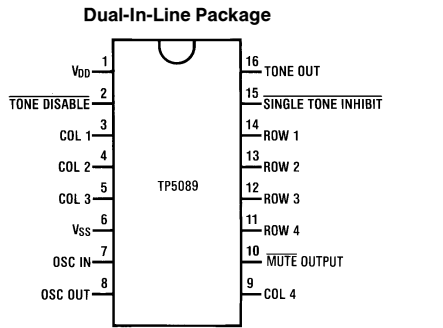
**Electrical Characteristics** Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for  $V_{DD} = 3.5V$  to  $10V$ ,  $T_A = 0^{\circ}C$  to  $+60^{\circ}C$  by correlation with 100% electrical testing at  $T_A = 25^{\circ}C$ . All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage for Keysense and MUTE Logic Functions		2			V
Minimum Operating Voltage for generating tones		<b>3.5</b>			V
Operating Current Idle Generating Tones	Mute open $R_L = \infty$ $V_{DD} = 3.5V$		2 1.1	<b>25</b> <b>2.5</b>	$\mu A$ mA
Input Resistors COLUMN and ROW (Pull-Up) SINGLE TONE INHIBIT (Pull-Down) TONE DISABLE (Pull-Up)		25 120	50		k $\Omega$ k $\Omega$
Input Low Level				<b>0.2 <math>V_{DD}</math></b>	V
Input High Level		<b>0.8 <math>V_{DD}</math></b>			V
MUTE OUT Sink Current (COLUMN and ROW Active)	$V_{DD} = 3.5V$ $V_o = 0.5V$	<b>0.4</b>			mA
MUTE Out Leakage Current	$V_o = V_{DD}$		1		$\mu A$
Output Amplitude Low Group	$R_L = 240\ \Omega$ $V_{DD} = 3.5V$	<b>190</b>	250	<b>340</b>	mVrms
	$R_L = 240\ \Omega$ $V_{DD} = 10V$	<b>510</b>	700	<b>880</b>	mVrms
Output Amplitude High Group	$R_L = 240\ \Omega$ $V_{DD} = 3.5V$	<b>270</b>	340	<b>470</b>	mVrms
	$R_L = 240\ \Omega$ $V_{DD} = 10V$	<b>735</b>	955	<b>1265</b>	mVrms
Mean Output DC Offset	$V_{DD} = 3.5V$ $V_{DD} = 10V$		1.3 4.6		V V
High Group Pre-Emphasis		<b>2.2</b>	2.7	<b>3.2</b>	dB
Dual Tone/Total Harmonic Distortion Ratio	$V_{DD} = 4V$ , $R_L = 240\ \Omega$ 1 MHz Bandwidth		-23	<b>-22</b>	dB
Start-Up Time (to 90% Amplitude)			3	5	mS

**Note 1:**  $R_L$  is the external load resistor connected from TONE OUT to  $V_{SS}$ .

**Note 2:** Crystal specification: Parallel resonant 3.579545 MHz,  $R_S \leq 150\ \Omega$ ,  $L = 100\ mH$ ,  $C_O = 5\ pF$ ,  $C_I = 0.02\ pF$ .

## Connection Diagram



Top View

Order Number TP5089N  
See NS Package N16A

TL/H/5057-2

## Pin Descriptions

Symbol	Description
$V_{DD}$	This is the positive voltage supply to the device, referenced to $V_{SS}$ . The collector of the TONE OUT transistor is connected to this pin.
$V_{SS}$	This is the negative voltage supply. All voltages are referenced to this pin.
OSC IN, OSC OUT	All tone generation timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when column inputs are sensed with no valid input having been detected. The oscillator is also stopped when the TONE DISABLE input is pulled to logic low.
Row and Column Inputs	When no key is pushed, pull-up resistors are active on row and column inputs. A key closure is recognized when a single row and a single column are connected to $V_{SS}$ , which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.
$\overline{\text{TONE DISABLE}}$ Input	The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, TONE OUT will be at an open circuit state.

## Symbol

MUTE Output

$\overline{\text{SINGLE TONE INHIBIT}}$  Input

TONE OUT

## Description

The MUTE output is an open-drain N-channel device that sinks current to  $V_{SS}$  with any key input and is open when no key input is sensed. The  $\overline{\text{MUTE}}$  output will switch regardless of the state of the SINGLE TONE INHIBIT input.

The  $\overline{\text{SINGLE TONE INHIBIT}}$  input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-down resistor to  $V_{SS}$ , and when left open or tied to  $V_{SS}$  any input condition that would normally result in a single tone will now result in no tone, with all other functions operating normally. When tied to  $V_{DD}$ , single or dual tones may be generated, see Table II.

This output is the open emitter of an NPN transistor, the collector of which is connected to  $V_{DD}$ . When an external load resistor is connected from TONE OUT to  $V_{SS}$ , the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current.

Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sinewave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion.

## Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically. Any key closure activates the MUTE output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to  $V_{SS}$ . This resistor facilitates adjustment of the signal current flowing from  $V_{DD}$  through the output transistor.

The amplitude of the output tones is directly proportional to the device supply voltage.

## Functional Description (Continued)

**TABLE I. Output Frequency Accuracy**

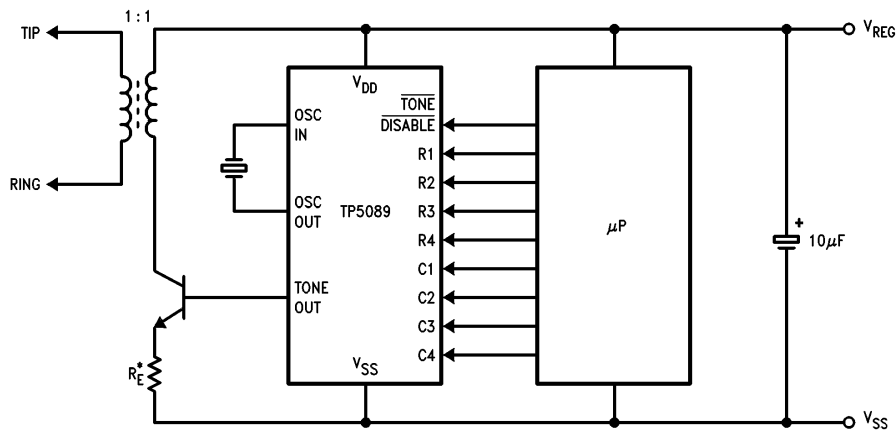
Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group $f_L$	R1	697	694.8	-0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	-0.11
High Group $f_H$	C1	1209	1206.0	-0.24
	C2	1336	1331.7	-0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

**TABLE II. Functional Truth Table**

SINGLE TONE INHIBIT	$\overline{\text{TONE DISABLE}}$	ROW	COLUMN	TONE OUT		MUTE
				Low	High	
X	0	O/C	O/C	0V	0V	O/C
X	X	O/C	O/C	0V	0V	O/C
X	0	One	One	$V_{OS}$	$V_{OS}$	0
X	1	One	One	$f_L$	$f_H$	0
1	1	2 or More	One	—	$f_H$	0
1	1	One	2 or More	$f_L$	—	0
1	1	2 or More	2 or More	$V_{OS}$	$V_{OS}$	0
0	1	2 or More	One	$V_{OS}$	$V_{OS}$	0
0	1	One	2 or More	$V_{OS}$	$V_{OS}$	0
0	1	2 or More	2 or More	$V_{OS}$	$V_{OS}$	0

**Note 1:** X is don't care state.

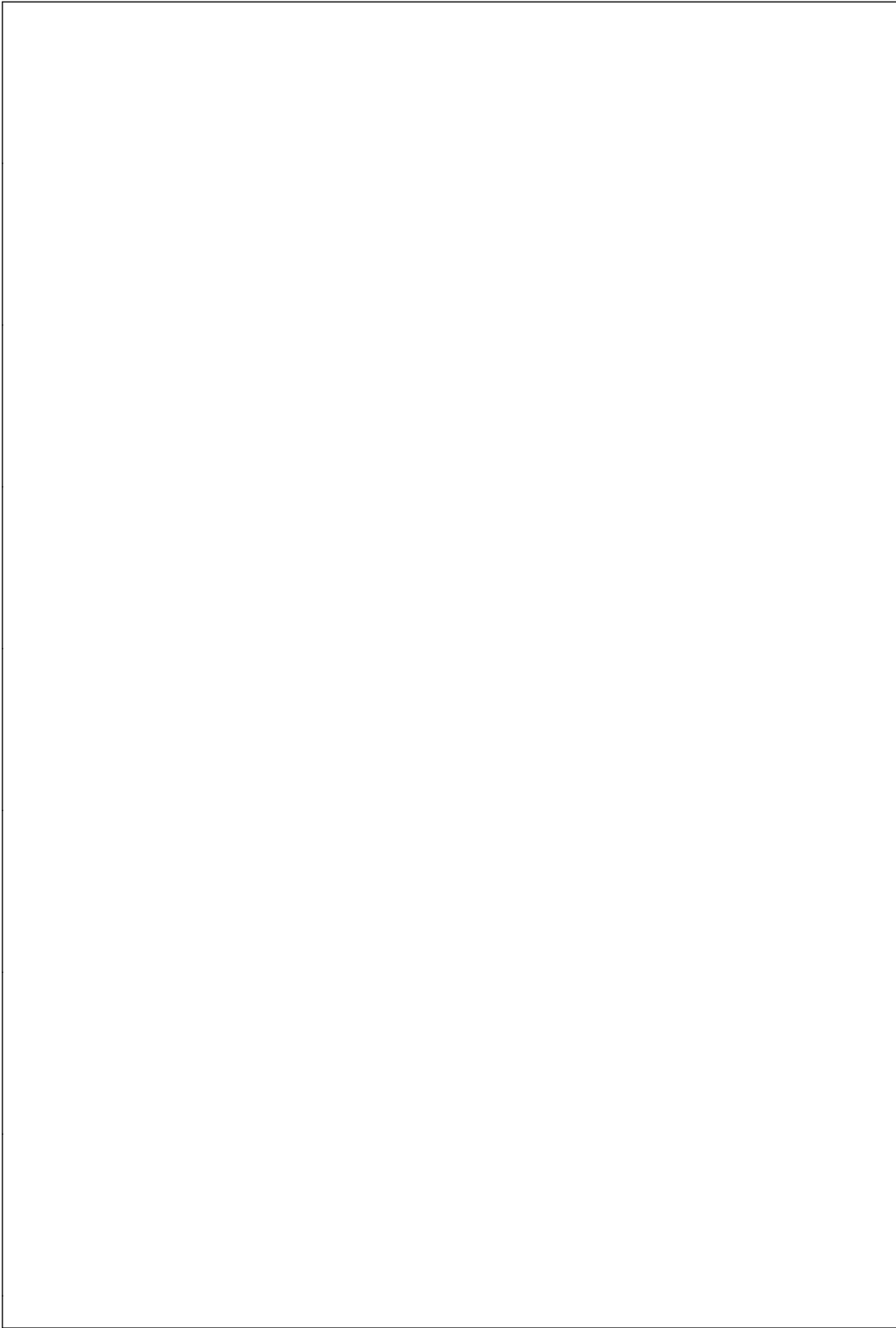
**Note 2:**  $V_{OS}$  is the output offset voltage.



\*Adjust  $R_E$  for desired tone amplitude.

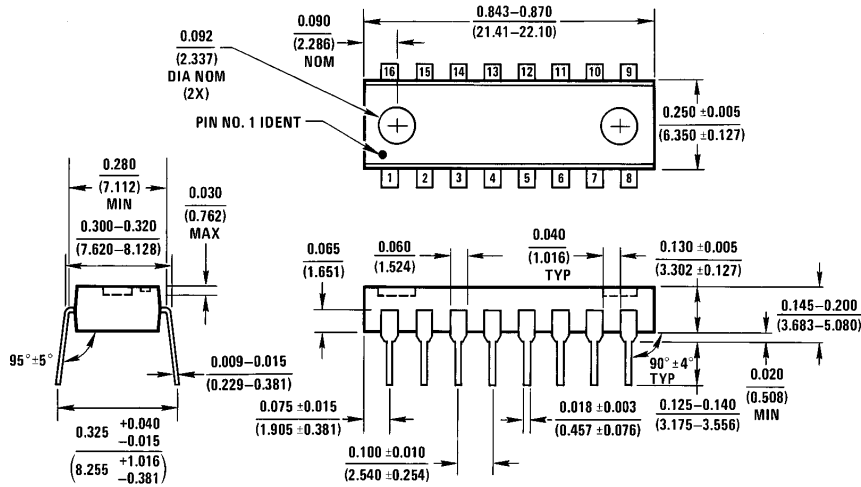
**FIGURE 2. Typical Application**

TL/H/5057-3



**Physical Dimensions** inches (millimeters)

Lit. # 113986



**Molded Dual-In-Line Package (N)**  
**Order Number TP5089N**  
**NS Package N16A**

N16A (REV E)

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