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Jameco Part Number 50534FSC

DM7473 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

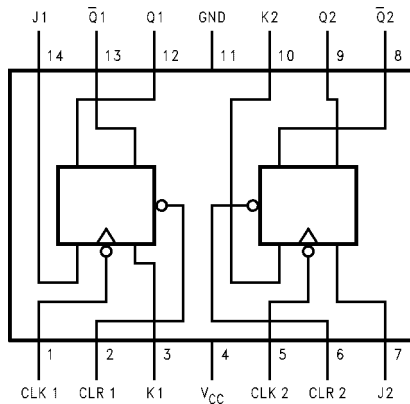
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is LOW the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is HIGH the J and K inputs are disabled. On the

negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is HIGH. Data transfers to the outputs on the falling edge of the clock pulse. A LOW logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| DM7473N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Connection Diagram



Function Table

| Inputs | | | | Outputs | |
|--------|-----|---|---|---------|-------------|
| CLR | CLK | J | K | Q | \bar{Q} |
| L | X | X | X | L | H |
| H | | L | L | Q_0 | \bar{Q}_0 |
| H | | H | L | H | L |
| H | | L | H | L | H |
| H | | H | H | Toggle | |

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

= Positive pulse data. the J and K inputs must be held constant while the clock is HIGH. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each HIGH level clock pulse.

Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|------------------|-----------------------------------|------------|-----|------|-------|
| V _{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} | HIGH Level Input Voltage | 2 | | | V |
| V _{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I _{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I _{OL} | LOW Level Output Current | | | 16 | mA |
| f _{CLK} | Clock Frequency (Note 3) | 0 | | 15 | MHz |
| t _W | Pulse Width (Note 3) | Clock HIGH | 20 | | ns |
| | | Clock LOW | 47 | | |
| | | Clear LOW | 25 | | |
| t _{SU} | Input Setup Time (Note 2)(Note 3) | 0↑ | | | ns |
| t _H | Input Hold Time (Note 2)(Note 3) | 0↓ | | | ns |
| T _A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 2: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 4) | Max | Units |
|-----------------|-----------------------------------|--|-------|--------------|------|-------|
| V _I | Input Clamp Voltage | V _{CC} = Min, I _I = -12 mA | | | -1.5 | V |
| V _{OH} | HIGH Level | V _{CC} = Min, I _{OH} = Max | 2.4 | 3.4 | | V |
| | Output Voltage | V _{IL} = Max, V _{IH} = Min | | | | |
| V _{OL} | LOW Level | V _{CC} = Min, I _{OL} = Max | | 0.2 | 0.4 | V |
| | Output Voltage | V _{IH} = Min, V _{IL} = Max | | | | |
| I _I | Input Current @ Max Input Voltage | V _{CC} = Max, V _I = 5.5V | | | 1 | mA |
| I _{IH} | HIGH Level Input Current | V _{CC} = Max V _I = 2.4V | J, K | | 40 | μA |
| | | | Clock | | 80 | |
| | | | Clear | | 80 | |
| I _{IL} | LOW Level Input Current | V _{CC} = Max V _I = 0.4V | J, K | | -1.6 | mA |
| | | | Clock | | -3.2 | |
| | | | Clear | | -3.2 | |
| I _{OS} | Short Circuit Output Current | V _{CC} = Max (Note 5) | -18 | | -55 | mA |
| I _{CC} | Supply Current | V _{CC} = Max, (Note 6) | | 18 | 34 | mA |

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

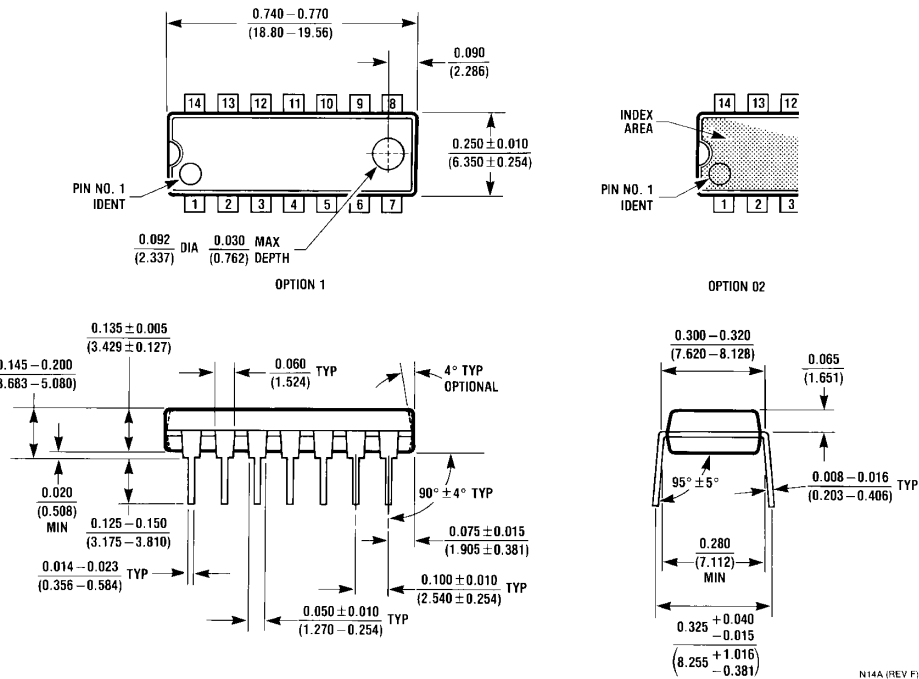
Note 5: Not more than one output should be shorted at a time.

Note 6: With all outputs OPEN, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn. At the time of measurement the clock input grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

| Symbol | Parameter | From (Input) To (Output) | R _L = 400Ω, C _L = 15 pF | | Units |
|------------------|---|-----------------------------|---|-----|-------|
| | | | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | | 15 | | MHz |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Q | | 40 | ns |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clear to \bar{Q} | | 25 | ns |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Q or \bar{Q} | | 40 | ns |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Q or \bar{Q} | | 25 | ns |

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

N14A (REV F)

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