National Semiconductor

DM5483/DM7483 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  Two 8-bit words 23 ns
  Two 16-bit words 43 ns
- Typical power dissipation per 4-bit adder 290 mW

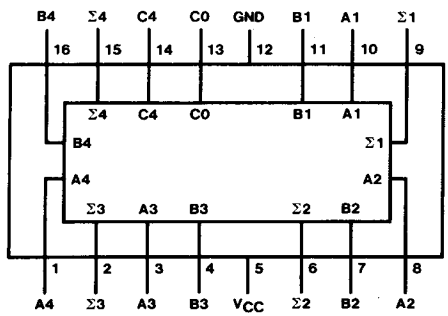
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6529-1

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6

Recommended Operating Conditions

Sym	Parameter	DM5483			DM7483			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current (Output C4)			−0.4			−0.4	mA
	High Level Output Current—Other Outputs			−0.8			−0.8	
I_{OL}	Low Level Output Current (Output C4)			8			8	mA
	Low Level Output Current—Other Outputs			16			16	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current (Output C4)	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
	Short Circuit Output Current (Other Outputs)	V_{CC} = Max (Note 2)	DM54	−20		−70	
			DM74	−18		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			58	79	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to $\Sigma1, \Sigma2$		20	32	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to $\Sigma1, \Sigma2$		22	32	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to $\Sigma3$		22	38	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to $\Sigma3$		28	47	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to $\Sigma4$		28	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to $\Sigma4$		28	47	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A_i, B_i to Σ_i			33	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A_i, B_i to Σ_i			38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	C0 to C4		12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	C0 to C4		12	19	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A_i, B_i to C4		12	19	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A_i, B_i to C4		12	19	ns

Function Table

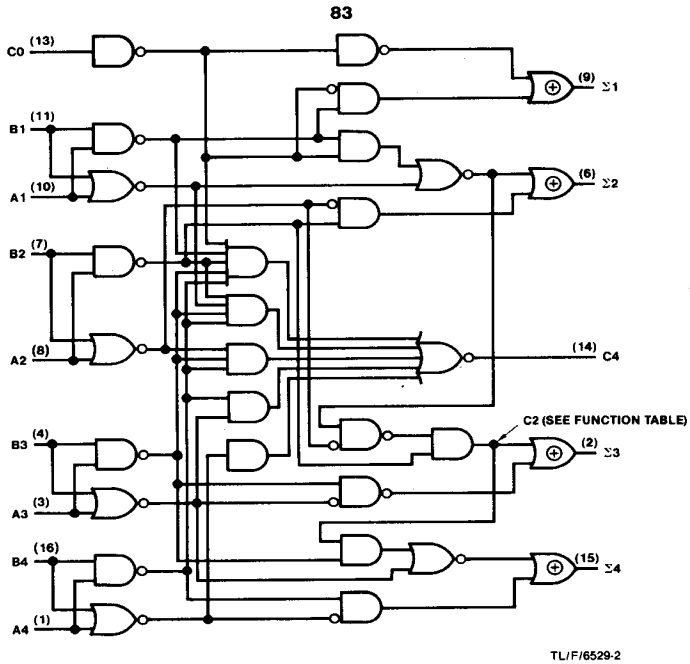
Input				Output							
				When C0 = L			When C0 = H				
						When C2 = L					When C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

Note

Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram



TL/F/6529-2