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# NEW HIGH PERFORMANCE ID8049/8039 SINGLE COMPONENT 8-BIT MICROCOMPUTER

- \*8049 Mask Programmable ROM
- \*8039 External ROM or EPROM
- \*6 MHz Operation

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|--|---|
| <ul style="list-style-type: none"> <li>■ 8-Bit CPU, ROM, RAM, I/O in Single Package</li> <li>■ Single 5V ± 10% Supply</li> <li>■ 2.5 μsec Cycle; All Instructions 1 or 2 Cycles</li> <li>■ Over 90 Instructions: 70% Single Byte</li> <li>■ Pin Compatible with 8048/8748</li> </ul> | <ul style="list-style-type: none"> <li>■ 2K × 8 ROM</li> <li>■ 128 × 8 RAM</li> <li>■ 27 I/O Lines</li> <li>■ Interval Timer/Event Counter</li> <li>■ Easily Expandable Memory and I/O</li> <li>■ Compatible with MCS Memory and I/O</li> <li>■ Single Level Interrupt</li> </ul> |
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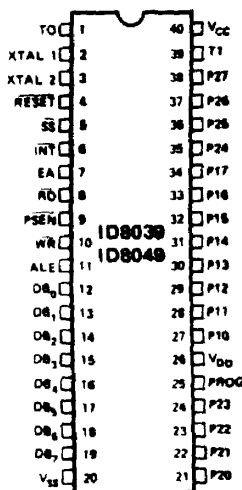
The Intel® ID8049/8039 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8049 contains a 2K × 8 program memory, a 128 × 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8049 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8039 is the equivalent to an 8049 without program memory.

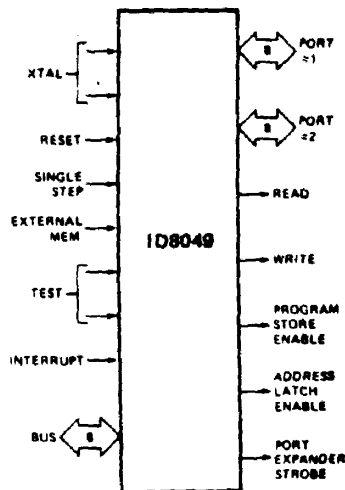
To reduce development problems to a minimum and provide maximum flexibility, two interchangeable pin-compatible versions of this single component microcomputer exist: the 8049 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8039 without program memory for use with external program memories in prototype and preproduction systems.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

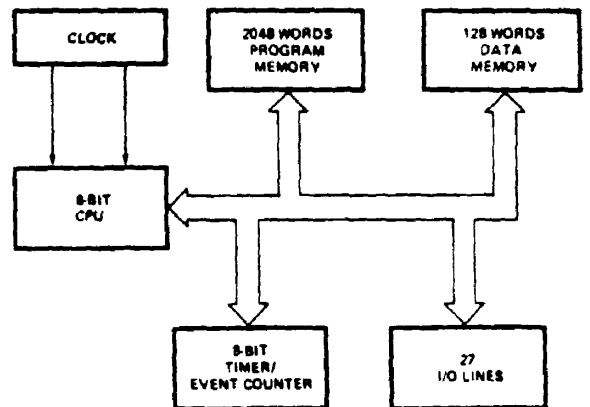
### PIN CONFIGURATION



### LOGIC SYMBOL



### BLOCK DIAGRAM



## PIN DESCRIPTION

Designation	Pin #	Function	Designation	Pin #	Function
V <sub>SS</sub>	20	Circuit GND potential	$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.  Used as a Read Strobe to External Data Memory. (Active low)
V <sub>DD</sub>	26	+5V during operation. Low power standby pin.	$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during verification, and power down. (Active low) (Non TTL V <sub>IH</sub> )
V <sub>CC</sub>	40	Main power supply; +5V during operation.	$\overline{WR}$	10	Output strobe during a BUS write. (Active low)  Used as write strobe to External Data Memory.
PROG	25	Output strobe for 8243 I/O expander.	ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.  The negative edge of ALE strobes address into external data and program memory.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.	$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243	$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
D0-D7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$ , $\overline{WR}$ strobes. The port can also be statically latched.  Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ , and $\overline{WR}$ .	EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.	XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.	XTAL2	3	Other side of crystal input.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)			

## INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle		Mnemonic	Description	Bytes	Cycle	
Accumulator	ADD A, R	Add register to A	1	1	Subroutine	CALL	Jump to subroutine	2	2	
	ADD A, @R	Add data memory to A	1	1		RET	Return	1	2	
	ADD A, #data	Add immediate to A	2	2		RETR	Return and restore status	1	2	
	ADDC A, R	Add register with carry	1	1		Flags	CLR C	Clear Carry	1	1
	ADDC A, @R	Add data memory with carry	1	1			CPL C	Complement Carry	1	1
	ADDC A, #data	Add immediate with carry	2	2	CLR F0		Clear Flag 0	1	1	
	ANL A, R	And register to A	1	1	CPL F0		Complement Flag 0	1	1	
	ANL A, @R	And data memory to A	1	1	CLR F1		Clear Flag 1	1	1	
	ANL A, #data	And immediate to A	2	2	CPL F1	Complement Flag 1	1	1		
	ORL A, R	Or register to A	1	1	Data Moves	MOV A, R	Move register to A	1	1	
	ORL A, @R	Or data memory to A	1	1		MOV A, @R	Move data memory to A	1	1	
	ORL A, #data	Or immediate to A	2	2		MOV A, #data	Move immediate to A	2	2	
	XRL A, R	Exclusive Or register to A	1	1		MOV R, A	Move A to register	1	1	
	XRL A, @R	Exclusive or data memory to A	1	1		MOV @R, A	Move A to data memory	1	1	
	XRL A, #data	Exclusive or immediate to A	2	2		MOV R, #data	Move immediate to register	2	2	
	INC A	Increment A	1	1		MOV @R, #data	Move immediate to data memory	2	2	
	DEC A	Decrement A	1	1		MOV A, PSW	Move PSW to A	1	1	
	CLR A	Clear A	1	1		MOV PSW, A	Move A to PSW	1	1	
	CPL A	Complement A	1	1		XCH A, R	Exchange A and register	1	1	
	DA A	Decimal Adjust A	1	1		XCH A, @R	Exchange A and data memory	1	1	
	SWAP A	Swap nibbles of A	1	1		XCHD A, @R	Exchange nibble of A and register	1	1	
	RL A	Rotate A left	1	1		MOVX A, @R	Move external data memory to A	1	2	
	RLC A	Rotate A left through carry	1	1		MOVX @R, A	Move A to external data memory	1	2	
	RR A	Rotate A right	1	1		MOV P, A	Move to A from current page	1	2	
	RRC A	Rotate A right through carry	1	1	MOV P3 A, @A	Move to A from Page 3	1	2		
	Input/Output	IN A, P	Input port to A	1	2	Timer/Counter	MOV A, T	Read Timer/Counter	1	1
		OUTL P, A	Output A to port	1	2		MOV T, A	Load Timer/Counter	1	1
		ANL P, #data	And immediate to port	2	2		STRT T	Start Timer	1	1
ORL P, #data		Or immediate to port	2	2	STRT CNT		Start Counter	1	1	
INS A, BUS		Input BUS to A	1	2	STOP TCNT		Stop Timer/Counter	1	1	
OUTL BUS, A		Output A to BUS	1	2	EN TCNTI		Enable Timer/Counter Interrupt	1	1	
ANL BUS, #data		And immediate to BUS	2	2	DIS TCNTI		Disable Timer/Counter Interrupt	1	1	
ORL BUS, #data		Or immediate to BUS	2	2	Control	ENI	Enable external interrupt	1	1	
MOVD A, P		Input Expander port to A	1	2		DISI	Disable external interrupt	1	1	
MOVD P, A		Output A to Expander port	1	2		SEL RB0	Select register bank 0	1	1	
ANLD P, A	And A to Expander port	1	2	SEL RB1		Select register bank 1	1	1		
ORLD P, A	Or A to Expander port	1	2	SEL MB0		Select memory bank 0	1	1		
Registers	INC R	Increment register	1	1	SEL MB1	Select memory bank 1	1	1		
	INC @R	Increment data memory	1	1	ENT0 CLK	Enable Clock output on T0	1	1		
	DEC R	Decrement register	1	1	Branch	NOP	No Operation	1	1	
	JMP addr	Jump unconditional	2	2						
	JMPP @A	Jump indirect	1	2						
DJNZ R, addr	Decrement register and skip	2	2							
JC addr	Jump on Carry = 1	2	2							
JNC addr	Jump on Carry = 0	2	2							
JZ addr	Jump on A Zero	2	2							
JNZ addr	Jump on A not Zero	2	2							
JTO addr	Jump on T0 = 1	2	2							
JNT0 addr	Jump on T0 = 0	2	2							
JT1 addr	Jump on T1 = 1	2	2							
JNT1 addr	Jump on T1 = 0	2	2							
JF0 addr	Jump on F0 = 1	2	2							
JF1 addr	Jump on F1 = 1	2	2							
JTF addr	Jump on timer flag	2	2							
JNI addr	Jump on INT = 0	2	2							
JBb addr	Jump on Accumulator Bit	2	2							

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**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5 Watt

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. AND OPERATING CHARACTERISTICS**  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ 

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
$V_{IL}$	Input Low Voltage	-0.5		0.6	V	
$V_{IH}$	Input High Voltage (All Except XTAL1, XTAL2, RESET)	2.2		$V_{CC}$	V	
$V_{IH1}$	Input High Voltage (RESET, X1, X2)	3.8		$V_{CC}$	V	
$V_{OL}$	Output Low Voltage (BUS, RD, WR, PSEN, ALE)			0.45	V	$I_{OL} = 1.6\text{ ma}$
$V_{OL1}$	Output Low Voltage (All Other Outputs Except PROG)			0.45	V	$I_{OL} = 1.2\text{ ma}$
$V_{OL2}$	Output Low Voltage (PROG)			0.45	V	$I_{OL} = 0.8\text{ ma}$
$V_{OH}$	Output High Voltage (BUS, RD, WR, PSEN, ALE)	2.4			V	$I_{OH} = -80\ \mu\text{a}$
$V_{OH1}$	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = -30\ \mu\text{a}$
$I_{IL}$	Input Leakage Current (T1, INT)			$\pm 10$	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{CC}$
$I_{OL}$	Output Leakage Current (Bus, T0) (High Impedance State)			$\pm 10$	$\mu\text{A}$	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
$I_{DD}$	Power Down Supply Current			50	mA	$T_A = 25^\circ\text{C}$
$I_{DD} + I_{CC}$	Total Supply Current			170	mA	$T_A = 25^\circ\text{C}$

**A.C. CHARACTERISTICS**  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = V_{DD} = +5V \pm 10\%$ ,  $V_{SS} = 0V$ 

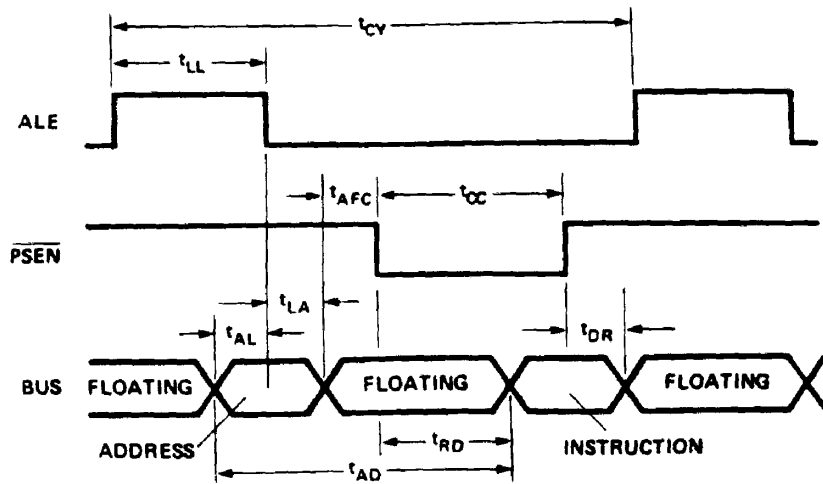
Symbol	Parameter	Min.	Max.	Unit	Conditions (Note 2)
$t_{LL}$	ALE Pulse Width	200		ns	
$t_{AL}$	Address Setup to ALE	120		ns	
$t_{LA}$	Address Hold from ALE	80		ns	
$t_{CC}$	Control Pulse Width (PSEN, RD, WR)	400		ns	
$t_{DW}$	Data Set-Up Before WR	420		ns	
$t_{WD}$	Data Hold After WR	80		ns	$C_L = 20\text{pF}$
$t_{CY}$	Cycle Time	2.5	15.0	$\mu\text{s}$	(6 MHz XTAL for ID8049)
$t_{DR}$	Data Hold	0	200	ns	
$t_{RD}$	PSEN, RD to Data In		400	ns	
$t_{AW}$	Address Setup to WR	230		ns	
$t_{AD}$	Address Setup to Data In		600	ns	
$t_{AFC}$	Address Float to RD, PSEN	-40		ns	

Notes: 1. 8039-6 specifications are also valid for 8049/8039 operating at 6MHz.

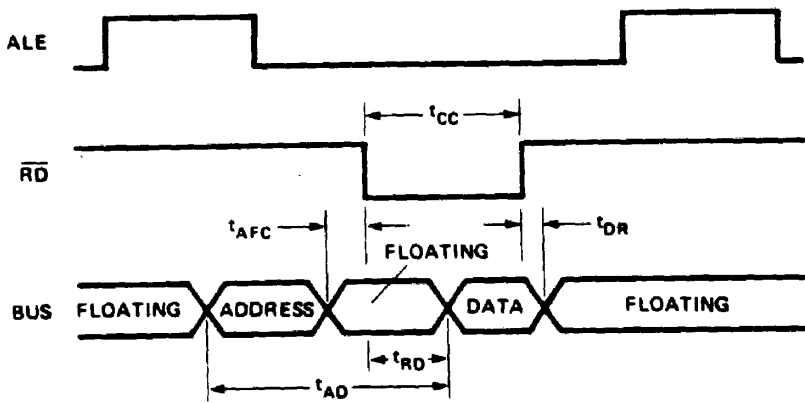
2. Control Outputs:  $C_L = 80\text{pF}$   
 BUS Outputs:  $C_L = 150\text{pF}$

WAVEFORMS

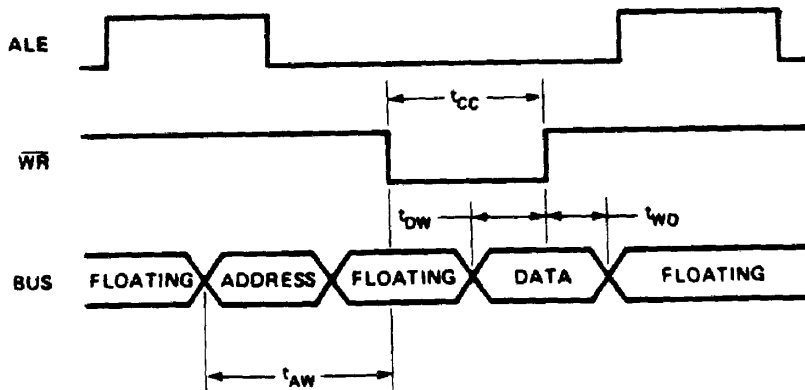
INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY



### A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Max.	Unit	Conditions (Note 2)
$t_{CP}$	Port Control Setup Before Falling Edge of PROG	115		ns	
$t_{PC}$	Port Control Hold After Falling Edge of PROG	65		ns	
$t_{PR}$	PROG to Time P2 Input Must Be Valid		860	ns	
$t_{OP}$	Output Data Setup Time	230		ns	
$t_{OH}$	Output Data Hold Time	25		ns	
$t_{IH}$	Input Data Hold Time	0	160	ns	
$t_{PW}$	PROG Pulse Width	920		ns	
$t_{PI}$	Port 2 I/O Data Setup	300		ns	
$t_{PH}$	Port 2 I/O Data Hold	120		ns	

### WAVEFORMS

#### PORT 2 TIMING

