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# 8224 CLOCK GENERATOR AND DRIVER FOR 8080A CPU

- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count
- Available in EXPRESS — Standard Temperature Range
- Available in 16-Lead Cerdip Package  
(See Packaging Spec, Order #231369)

The Intel 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

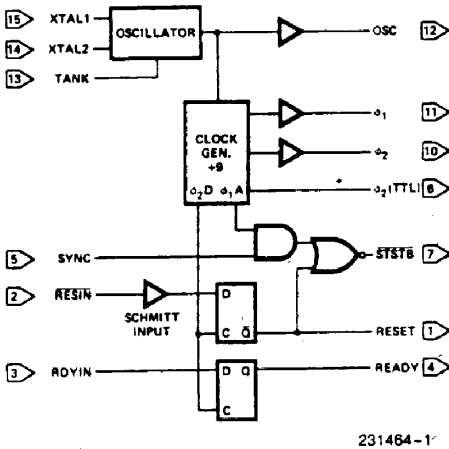
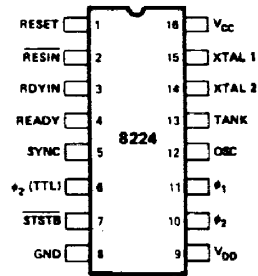


Figure 1. Block Diagram



RESIN	Reset Input	XTAL 1	} Connections for Crystal
RESET	Reset Output	XTAL 2	
RDYIN	Ready input	TANK	Used with Overtone XTAL
READY	Ready Output	OSC	Oscillator Output
SYNC	Sync Input	phi_2 (TTL)	phi_2 CLK (TTL Level)
STSTB	Status STB (Active Low)	V <sub>CC</sub>	+5V
phi_1	} 8080 Clocks	V <sub>DD</sub>	+12V
phi_2		GND	0V

Figure 2. Pin Configuration

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias ..... 0°C to +70°C  
 Storage Temperature ..... -65°C to +150°C  
 Supply Voltage, V<sub>CC</sub> ..... -0.5V to +7V  
 Supply Voltage, V<sub>DD</sub> ..... -0.5V to +13.5V  
 Input Voltage ..... -1.5V to +7V  
 Output Current ..... 100 mA

*\*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**D.C. CHARACTERISTICS**

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +5.0V ±5%, V<sub>DD</sub> = +12V ±5%

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I <sub>F</sub>	Input Current Loading			-0.25	mA	V <sub>F</sub> = 0.45V
I <sub>R</sub>	Input Leakage Current			10	μA	V <sub>R</sub> = 5.25V
V <sub>C</sub>	Input Forward Clamp Voltage			1.0	V	I <sub>C</sub> = -5 mA
V <sub>IL</sub>	Input "Low" Voltage			0.8	V	V <sub>CC</sub> = 5.0V
V <sub>IH</sub>	Input "High" Voltage	2.6			V	Reset Input
		2.0			V	All Other Inputs
V <sub>IH</sub> -V <sub>IL</sub>	RESIN Input Hysteresis	0.25			V	V <sub>CC</sub> = 5.0V
V <sub>OL</sub>	Output "Low" Voltage			0.45	V	(φ <sub>1</sub> , φ <sub>2</sub> ), Ready, Reset, STSTB I <sub>OL</sub> = 2.5 mA
				0.45	V	All Other Outputs I <sub>OL</sub> = 15 mA
V <sub>OH</sub>	Output "High" Voltage φ <sub>1</sub> , φ <sub>2</sub>	9.4			V	I <sub>OH</sub> = -100 μA
	READY, RESET	3.6			V	I <sub>OH</sub> = -100 μA
	All Other Outputs	2.4			V	I <sub>OH</sub> = -1 mA
I <sub>CC</sub>	Power Supply Current			115	mA	
I <sub>DD</sub>	Power Supply Current			12	mA	

**NOTE:**

1. For crystal frequencies of 18 MHz connect 510Ω resistors between the X1 input and ground as well as the X2 input and ground to prevent oscillation at harmonic frequencies.

**Crystal Requirements**

Tolerance: 0.005% at 0°C-70°C  
 Resonance: Series (Fundamental)\*  
 Load Capacitance: 20 pF-35 pF  
 Equivalent Resistance: 75Ω-20Ω

Power Dissipation (Min): 4 mW

**\*NOTE:**

With tank circuit use 3rd overtone mode.

**A.C. CHARACTERISTICS**

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$t_{\phi 1}$	$\phi_1$ Pulse Width	$\frac{2tcy}{9} - 20$ ns			ns	$C_L = 20$ pF to $50$ pF
$t_{\phi 2}$	$\phi_2$ Pulse Width	$\frac{5tcy}{9} - 35$ ns				
$t_{D1}$	$\phi_1$ to $\phi_2$ Delay	0				
$t_{D2}$	$\phi_2$ to $\phi_1$ Delay	$\frac{2tcy}{9} - 14$ ns				
$t_{D3}$	$\phi_1$ to $\phi_2$ Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9} + 20$ ns		
$t_R$	$\phi_1$ and $\phi_2$ Rise Time			20		
$t_F$	$\phi_1$ and $\phi_2$ Fall Time			20		
$t_{D\phi 2}$	$\phi_2$ to $\phi_2$ (TTL) Delay	-5		+15	ns	$\phi_2$ TTL, $C_L = 30$ $R_1 = 300\Omega$ $R_2 = 600\Omega$
$t_{DSS}$	$\phi_2$ to $\overline{STSTB}$ Delay	$\frac{6tcy}{9} - 30$ ns		$\frac{6tcy}{9}$	ns	$\overline{STSTB}$ , $C_L = 15$ pF $R_1 = 2K$ $R_2 = 4K$
$t_{PW}$	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9} - 15$ ns			ns	
$t_{DRS}$	RDYIN Setup Time to Status Strobe	$50$ ns - $\frac{4tcy}{9}$				
$t_{DRH}$	RDYIN Hold Time after $\overline{STSTB}$	$\frac{4tcy}{9}$				
$t_{DR}$	RDYIN or RESIN to $\phi_2$ Delay	$\frac{4tcy}{9} - 25$ ns			ns	Ready & Reset $C_L = 10$ pF $R_1 = 2K$ $R_2 = 4K$
$t_{CLK}$	CLK Period		$\frac{tcy}{9}$		ns	
$f_{max}$	Maximum Oscillating Frequency			27	MHz	
$C_{in}$	Input Capacitance			8	pF	$V_{CC} = +5.0V$ $V_{DD} = +12V$ $V_{BIAS} = 2.5V$ $f = 1$ MHz

**NOTE:**

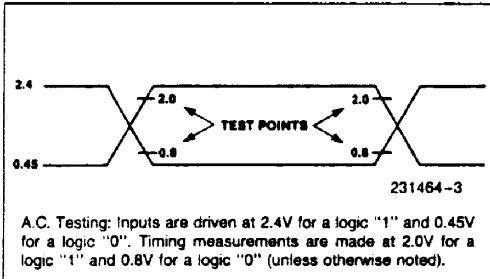
These formulas are based on the internal workings of the part and intended for customer convenience. Actual testing of the part is done at  $t_{cy} = 488.28$  ns.

**A.C. CHARACTERISTICS** (Continued)

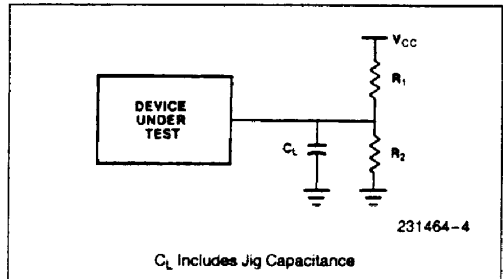
For  $t_{CY} = 488.28 \text{ ns}$ ;  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{DD} = +12\text{V} \pm 5\%$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
$t_{\phi 1}$	$\phi_1$ Pulse Width	89			ns	$t_{CY} = 488.28 \text{ ns}$  $\phi_1$ & $\phi_2$ Loaded to $C_L = 20 \text{ pF}$ to $50 \text{ pF}$  Ready & Reset Loaded to $2 \text{ mA}/10 \text{ pF}$ All measurements referenced to $1.5\text{V}$ unless specified otherwise.
$t_{\phi 2}$	$\phi_2$ Pulse Width	236			ns	
$t_{D1}$	Delay $\phi_1$ to $\phi_2$	0			ns	
$t_{D2}$	Delay $\phi_2$ to $\phi_1$	95			ns	
$t_{D3}$	Delay $\phi_1$ to $\phi_2$ Leading Edges	109		129	ns	
$t_r$	Output Rise Time			20	ns	
$t_f$	Output Fall Time			20	ns	
$t_{DSS}$	$\phi_2$ to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	$\phi_2$ to $\phi_2$ (TTL) Delay	-5		+15	ns	
$t_{PW}$	Status Strobe Pulse Width	40			ns	
$t_{DRS}$	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	
$t_{DRH}$	RDYIN Hold Time after $\overline{STSTB}$	217			ns	
$t_{DR}$	READY or RESET to $\phi_2$ Delay	192			ns	
$f_{MAX}$	Oscillator Frequency			18.432	MHz	

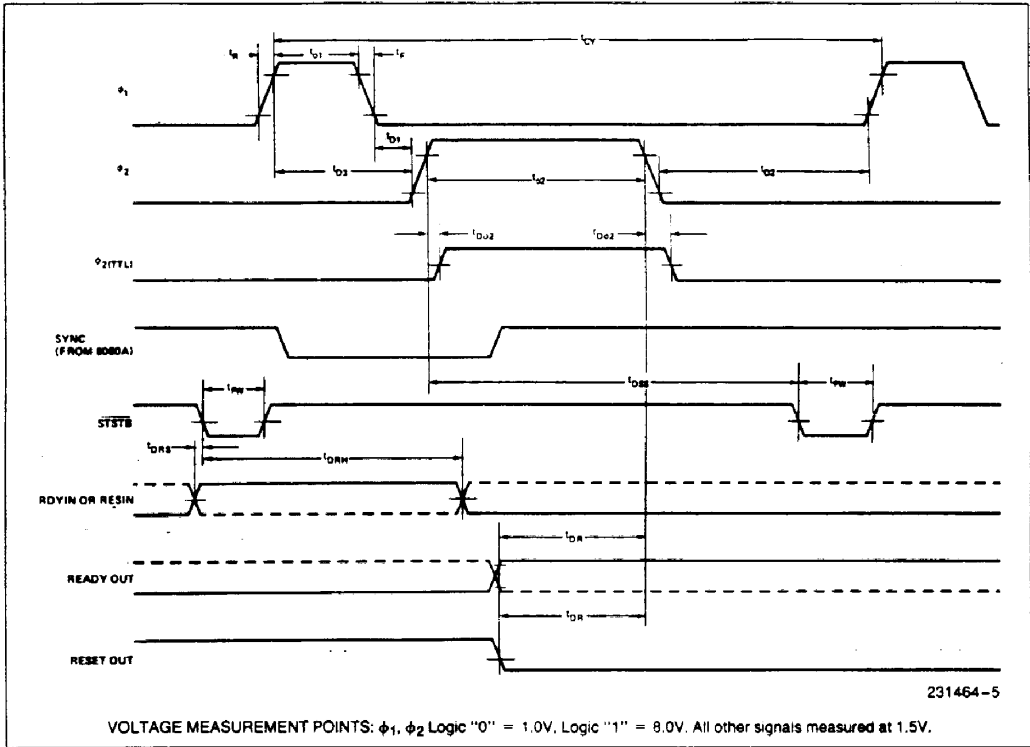
**A.C. TESTING, INPUT, OUTPUT WAVEFORM**



**A.C. TESTING LOAD CIRCUIT**



WAVEFORMS



CLOCK HIGH AND LOW TIME (USING X1, X2)

