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TYPES 1N4728 THRU 1N4752, 1N4728A THRU 1N4752A SILICON VOLTAGE-REGULATOR DIODES

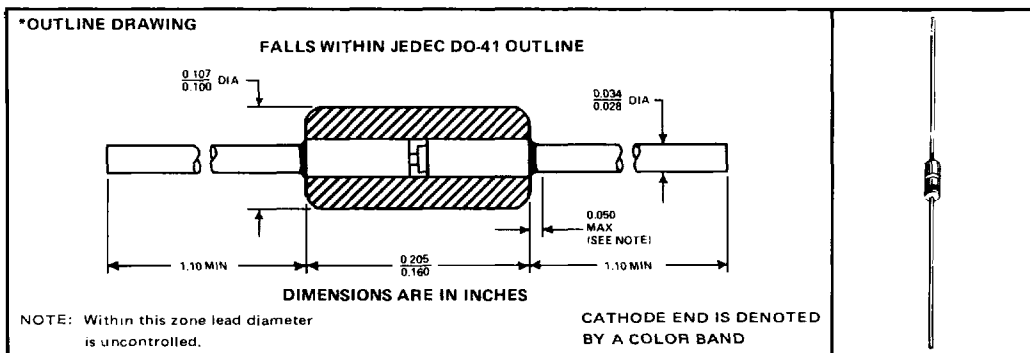
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$V_Z \dots 3.3 \text{ V to } 33 \text{ V}$
 $P_D \dots 1 \text{ W}$

- Available in 5% and 10% Tolerances
- Rugged Double-Plug Construction

mechanical data

These voltage regulator diodes have been designed using the best of both silicon material processing and packaging technologies. The silicon die is a planar oxide-passivated structure which has additional true-glass passivation over the junction. The double-plug package, proven by years of volume production, ensures the best in mechanical integrity and the lowest possible junction temperature when compared to the thermal characteristics of whisker packages.



absolute maximum ratings at specified free-air temperature (unless otherwise noted)

- *Steady-State Regulator Current, I_{ZM} , at (or below) 50°C (See Note 1) See Table 1
- *Nonrepetitive Reverse Surge Current, I_{RSM} , at (or below) 25°C (See Note 2) See Table 1
- *Continuous Power Dissipation at (or below) 50°C (See Note 3) 1 W
- *Operating Free-Air Temperature Range -65°C to 200°C
- Storage Temperature Range -65°C to 200°C
- *Lead Temperature 1/16 Inch from Case for 10 Seconds 230°C

TABLE 1—CURRENT RATINGS

TYPE	I_{ZM} (mA)	I_{RSM} (mA)	TYPE	I_{ZM} (mA)	I_{RSM} (mA)	TYPE	I_{ZM} (mA)	I_{RSM} (mA)
1N4728, A	276	1380	1N4738, A	110	550	1N4748, A	41	205
1N4729, A	252	1260	1N4739, A	100	500	1N4749, A	38	190
1N4730, A	234	1190	1N4740, A	91	454	1N4750, A	34	170
1N4731, A	217	1070	1N4741, A	83	414	1N4751, A	30	150
1N4732, A	193	970	1N4742, A	76	380	1N4752, A	27	135
1N4733, A	178	890	1N4743, A	69	344			
1N4734, A	162	810	1N4744, A	61	304			
1N4735, A	146	730	1N4745, A	57	285			
1N4736, A	133	660	1N4746, A	50	250			
1N4737, A	121	605	1N4747, A	45	225			

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- NOTES: 1. The nominal I_{ZM} currents shown are applicable for devices having regulator voltages approximately 10% above the nominal V_Z values shown under electrical characteristics. These values do not represent absolute limits. The actual steady-state current-voltage product must not exceed the power rating.
2. These values apply for an 8.3-ms square-wave pulse superposed on a steady-state reverse current equal to $I_{Z(T)}$ as shown under electrical characteristics.
3. Derate linearly to 200°C at the rate of $6.67 \text{ mW}/^\circ\text{C}$. See Figure 1.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

TYPES 1N4728 THRU 1N4752, 1N4728A THRU 1N4752A SILICON VOLTAGE-REGULATOR DIODES

*electrical characteristics at 25°C free-air temperature

CHARACTERISTICS						TEST CURRENT AND VOLTAGE		
PARAMETER	V _Z Regulator Voltage	Z _Z Small-Signal Regulator Impedance	Z _{ZK} Small-Signal Regulator Knee Impedance	I _R Static Reverse Current	V _F Static Forward Voltage			
TEST CONDITIONS	I _R = I _{Z(T)}	I _R = I _{Z(T)} , I _r = 10% I _{Z(T)} , f = 60 Hz	I _R = I _{ZK} , I _r = 10% I _{ZK} , f = 60 Hz	V _R = V _{R(T)}	I _F = 200 mA			
LIMIT	NOM [†]	MAX	MAX	MAX	MAX			
UNIT	V	Ω	Ω	μA	V	mA	mA	V
1N4728, A	3.3	10	400	100	1.2	76	1	1
1N4729, A	3.6	10	400	100	1.2	69	1	1
1N4730, A	3.9	9	400	50	1.2	64	1	1
1N4731, A	4.3	9	400	10	1.2	58	1	1
1N4732, A	4.7	8	500	10	1.2	53	1	1
1N4733, A	5.1	7	550	10	1.2	49	1	1
1N4734, A	5.6	5	600	10	1.2	45	1	2
1N4735, A	6.2	2	700	10	1.2	41	1	3
1N4736, A	6.8	3.5	700	10	1.2	37	1	4
1N4737, A	7.5	4.0	700	10	1.2	34	0.5	5
1N4738, A	8.2	4.5	700	10	1.2	31	0.5	6
1N4739, A	9.1	5	700	10	1.2	28	0.5	7
1N4740, A	10	7	700	10	1.2	25	0.25	7.6
1N4741, A	11	8	700	5	1.2	23	0.25	8.4
1N4742, A	12	9	700	5	1.2	21	0.25	9.1
1N4743, A	13	10	700	5	1.2	19	0.25	9.9
1N4744, A	15	14	700	5	1.2	17	0.25	11.4
1N4745, A	16	16	700	5	1.2	15.5	0.25	12.2
1N4746, A	18	20	750	5	1.2	14.0	0.25	13.7
1N4747, A	20	22	750	5	1.2	12.5	0.25	15.2
1N4748, A	22	23	750	5	1.2	11.5	0.25	16.7
1N4749, A	24	25	750	5	1.2	10.5	0.25	18.2
1N4750, A	27	35	750	5	1.2	9.5	0.25	20.6
1N4751, A	30	40	1000	5	1.2	8.5	0.25	22.8
1N4752, A	33	45	1000	5	1.2	7.5	0.25	25.1

[†]V_Z tolerance is ±10% for 1N4728 through 1N4752; ±5% for 1N4728A through 1N4752A.

THERMAL INFORMATION

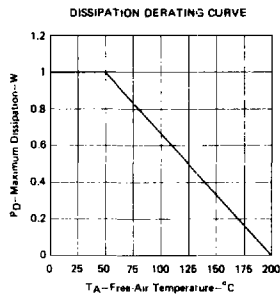


FIGURE 1

*JEDEC registered data