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Jameco Part Number 784642

74VHCT245A

Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHCT245A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHCT245A is intended for bidirectional asynchronous communication between data busses. The direction of data transmission is determined by the level of the T/R input. The enable input can be used to disable the device so that the busses are effectively isolated.

Protection circuits ensure that 0V to 7V can be applied to the input and output (Note 1) pins without regard to the supply voltage. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

Note 1: Outputs in OFF-State

Features

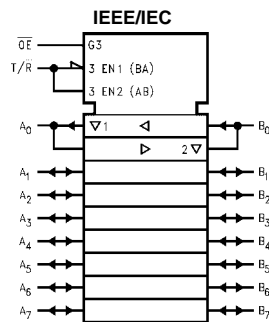
- High Speed: $t_{PD} = 5.4 \text{ ns (typ)}$ at $V_{CC} = 5V$
- Power Down Protection on Inputs and Outputs
- Low Power Dissipation: $I_{CC} = 4 \mu\text{A (Max)}$ @ $T_A = 25^\circ\text{C}$
- Pin and Function Compatible with 74HCT245

Ordering Code:

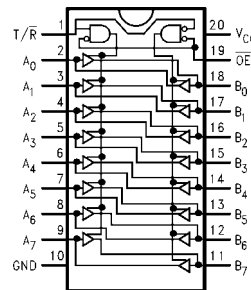
| Order Number | Package Number | Package Description |
|---------------|----------------|---|
| 74VHCT245AM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74VHCT245ASJ | M20D | Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74VHCT245AMTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74VHCT245AN | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



74VHCT245A Octal Buffer/Line Driver with 3-STATE Outputs

Pin Descriptions

| Pin Names | Description |
|--------------------------------|----------------------------------|
| \overline{OE} | Output Enable Input |
| $\overline{T/R}$ | Transmit/Receive Input |
| A ₀ -A ₇ | Side A Inputs or 3-STATE Outputs |
| B ₀ -B ₇ | Side B Inputs or 3-STATE Outputs |

Truth Table

| Inputs | | Outputs |
|-----------------|------------------|---------------------|
| \overline{OE} | $\overline{T/R}$ | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | HIGH-Z State |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Absolute Maximum Ratings (Note 2)

| | |
|---|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -0.5V to +7.0V |
| DC Output Voltage (V_{OUT}) (Note 3) | -0.5V to $V_{CC} + 0.5V$ |
| (Note 4) | -0.5V to +7.0V |
| Input Diode Current (I_{IK}) | -20 mA |
| Output Diode Current (I_{OK}) (Note 5) | ± 20 mA |
| DC Output Current (I_{OUT}) | ± 25 mA |
| DC V_{CC}/GND Current (I_{CC}) | ± 75 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Lead Temperature (T_L) (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 6)

| | |
|---|------------------|
| Supply Voltage (V_{CC}) | 4.5V to +5.5V |
| Input Voltage (V_{IN}) | 0V to +5.5V |
| Output Voltage (V_{OUT}) (Note 3) | 0V to V_{CC} |
| (Note 4) | 0V to +5.5V |
| Operating Temperature (T_{OPR}) | -40°C to +85°C |
| Input Rise and Fall Time (t_r, t_f) $V_{CC} = 5.0V \pm 0.5V$ | 0 ns/V ~ 20 ns/V |

Note 2: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 3: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

Note 4: When outputs are in OFF-State or when $V_{CC} = 0V$.

Note 5: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ (Outputs Active).

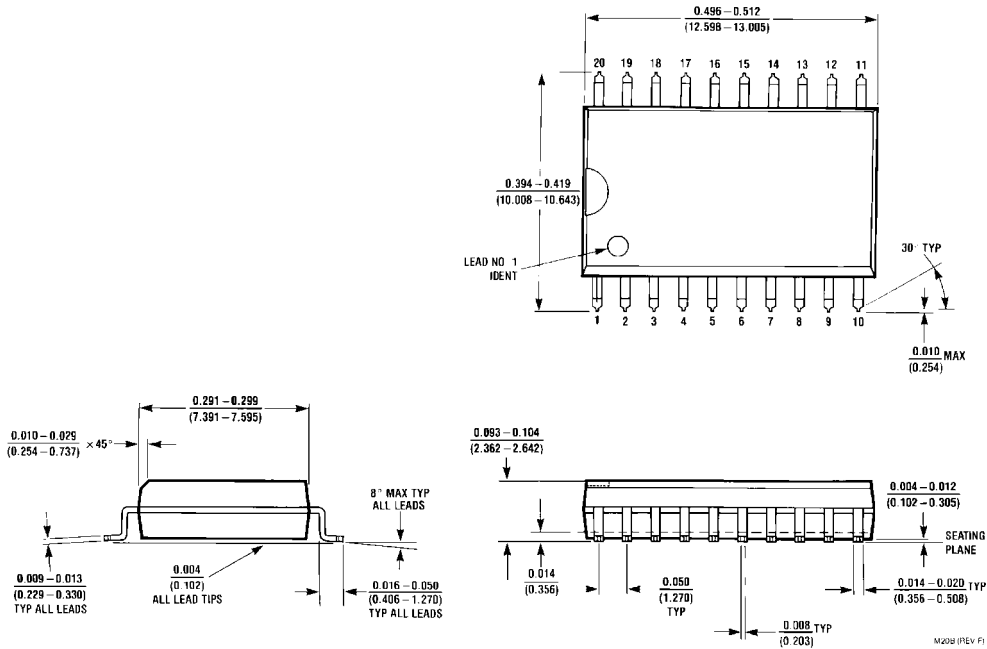
Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = 25^\circ C$ | | | $T_A = -40^\circ C$ to $+85^\circ C$ | | Units | Conditions |
|-----------|--|-----------------|--------------------|------------|-----|--------------------------------------|-----|---------|--|
| | | | Min | Typ | Max | Min | Max | | |
| V_{IH} | HIGH Level | 4.5 | 2.0 | | | 2.0 | | V | |
| | Input Voltage | 5.5 | 2.0 | | | 2.0 | | | |
| V_{IL} | LOW Level | 4.5 | | | 0.8 | | 0.8 | V | |
| | Input Voltage | 5.5 | | | 0.8 | | 0.8 | | |
| V_{OH} | HIGH Level | 4.5 | 4.40 | 4.50 | | 4.40 | | V | $V_{IN} = V_{IH}$ $I_{OH} = -50 \mu A$ |
| | Output Voltage | | 3.94 | | | 3.80 | | V | or V_{IL} $I_{OH} = -8 mA$ |
| V_{OL} | LOW Level | 4.5 | 0.0 | 0.1 | | 0.1 | | V | $V_{IN} = V_{IH}$ $I_{OL} = 50 \mu A$ |
| | Output Voltage | | | 0.36 | | 0.44 | | V | or V_{IL} $I_{OL} = 8 mA$ |
| I_{OZ} | 3-STATE Output Off-State Current | 5.5 | | ± 0.25 | | ± 2.5 | | μA | $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND |
| I_{IN} | Input Leakage Current | 0-5.5 | | ± 0.1 | | ± 1.0 | | μA | $V_{IN} = 5.5V$ or GND |
| I_{CC} | Quiescent Supply Current | 5.5 | | 4.0 | | 40.0 | | μA | $V_{IN} = V_{CC}$ or GND |
| I_{CCT} | Maximum $I_{CC}/Input$ | 5.5 | | 1.35 | | 1.50 | | mA | $V_{IN} = 3.4V$ Other Input = V_{CC} or GND |
| I_{OFF} | Output Leakage Current (Power Down State) | 0.0 | | 0.5 | | 5.0 | | μA | $V_{OUT} = 5.5V$ |

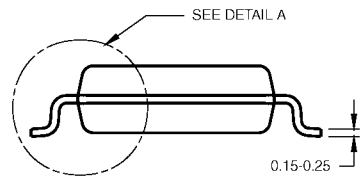
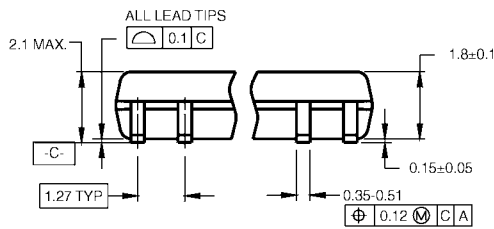
| Noise Characteristics | | | | | | | | | | |
|---|--|------------------------|-----------------------|--------|-------|---------------------------------|-----|------------------------|------------------------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | Units | Conditions | | | | |
| | | | Typ | Limits | | | | | | |
| V _{OLP} (Note 7) | Quiet Output Maximum Dynamic V _{OL} | 5.0 | 1.2 | 1.6 | V | C _L = 50 pF | | | | |
| V _{OLV} (Note 7) | Quiet Output Minimum Dynamic V _{OL} | 5.0 | -1.2 | -1.6 | V | C _L = 50 pF | | | | |
| V _{IHD} (Note 7) | Minimum HIGH Level Dynamic Input Voltage | 5.0 | | 2.0 | V | C _L = 50 pF | | | | |
| V _{ILD} (Note 7) | Maximum LOW Level Dynamic Input Voltage | 5.0 | | 0.8 | V | C _L = 50 pF | | | | |
| Note 7: Parameter guaranteed by design. | | | | | | | | | | |
| AC Electrical Characteristics | | | | | | | | | | |
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | T _A = -40°C to +85°C | | Units | Conditions | |
| | | | Min | Typ | Max | Min | Max | | | |
| t _{PLH} | Propagation Delay Time | 5.0 ± 0.5 | 4.9 | 7.7 | 1.0 | 8.5 | ns | | C _L = 15 pF | |
| t _{PHL} | | | 5.4 | 8.7 | 1.0 | 9.5 | | C _L = 50 pF | | |
| t _{PZL} | 3-STATE Output Enable Time | 5.0 ± 0.5 | 9.4 | 13.8 | 1.0 | 15.0 | ns | R _L = 1 kΩ | C _L = 15 pF | |
| t _{PZH} | | | 9.9 | 14.8 | 1.0 | 16.0 | | | C _L = 50 pF | |
| t _{PLZ} | 3-STATE Output Disable Time | 5.0 ± 0.5 | 10.1 | 15.4 | 1.0 | 16.5 | ns | R _L = 1 kΩ | C _L = 50 pF | |
| t _{PHZ} | | | | | | | | | | |
| t _{OSLH} | Output to Output Skew | 5.0 ± 0.5 | 1.0 | | 1.0 | | ns | (Note 8) | | |
| t _{OSHL} | | | | | | | | | | |
| C _{IN} | Input Capacitance | | 4 | 10 | 10 | | pF | V _{CC} = Open | | |
| C _{OUT} | Output Capacitance | | 13 | | | | pF | V _{CC} = 5.0V | | |
| C _{PD} | Power Dissipation Capacitance | | 16 | | | | pF | (Note 9) | | |
| Note 8: Parameter guaranteed by design. t _{OSLH} = t _{PLH max} - t _{PLH min} ; t _{OSHL} = t _{PHL max} - t _{PHL min} | | | | | | | | | | |
| Note 9: C _{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I _{CC (opr.)} = C _{PD} * V _{CC} * f _{IN} + I _{CC} /8 (per F/F). The total C _{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C _{PD (total)} = 20 + 12n. | | | | | | | | | | |

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

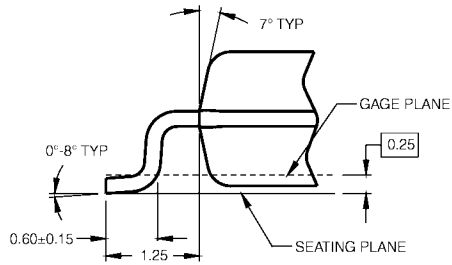


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1



DETAIL A

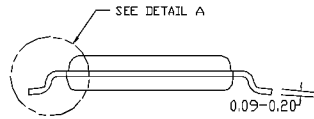
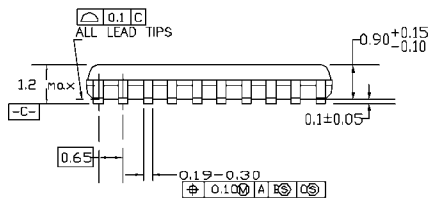
Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

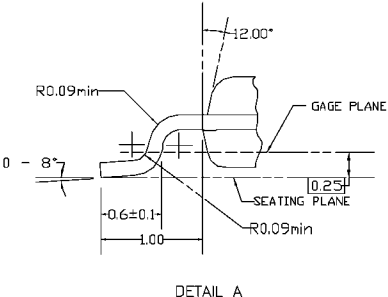


PIN #1 IDENT.

LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

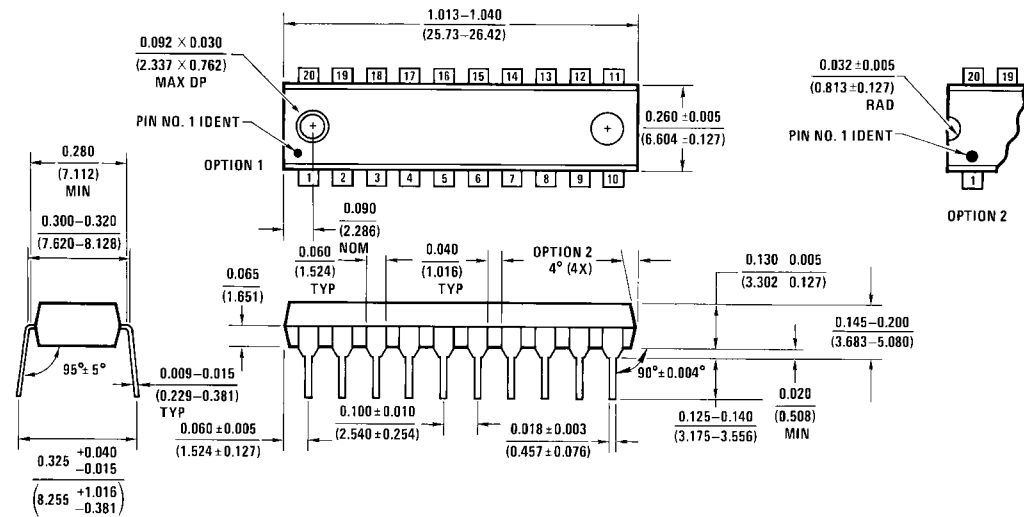


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
 - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

N20A (REV G)

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