

# Flip-flop

# FAST 74F175/175A

## Quad D flip-flop

### FEATURES

- Four edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- True and complementary outputs
- Industrial temperature range available (-40°C to +85°C)
- PNP light loading inputs ('F175A)
- Improved AC, DC, and functional ('F175A)

### DESCRIPTION

The 74F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and  $\bar{Q}$  outputs. The common buffered Clock (CP) and Master Reset ( $\bar{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. All Q outputs will be forced Low independently of clock or data inputs by Low voltage level on the  $\bar{MR}$  input. The device is useful for applications where both true and complementary outputs are required and the CP and  $\bar{MR}$  are common to all storage elements.

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	140MHz	25mA
74F175A	160MHz	22mA

### ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ $T_{amb} = 0^\circ C$ to $+70^\circ C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$ $T_{amb} = -40^\circ C$ to $+85^\circ C$
16-pin plastic DIP	N74F175N	IN74F175N
16-pin plastic SO	N74F175D	IN74F175D
16-pin plastic DIP	N74F175AN	IN74F175AN
16-pin plastic SO	N74F175AD	IN74F175AD

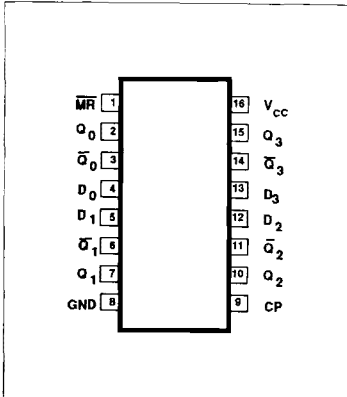
### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	'F175	1.0/1.0
		'F175A	1.0/0.033
$\bar{MR}$	Master Reset input (active Low)	'F175	1.0/1.0
		'F175A	1.0/0.033
CP	Clock Pulse input (active rising edge)	'F175	1.0/1.0
		'F175A	1.0/0.033
$Q_0 - Q_3$	True outputs	50/33	1.0mA/20mA
$\bar{Q}_0 - \bar{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

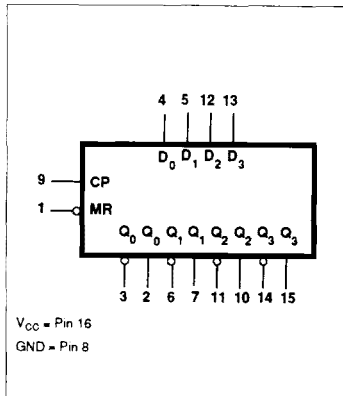
**NOTE:**

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

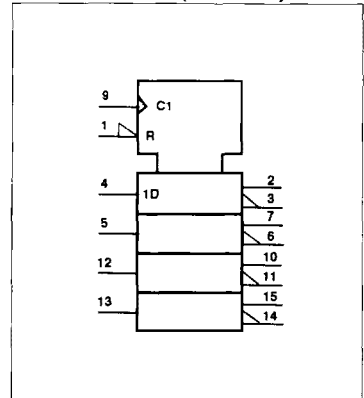
### PIN CONFIGURATION



### LOGIC SYMBOL



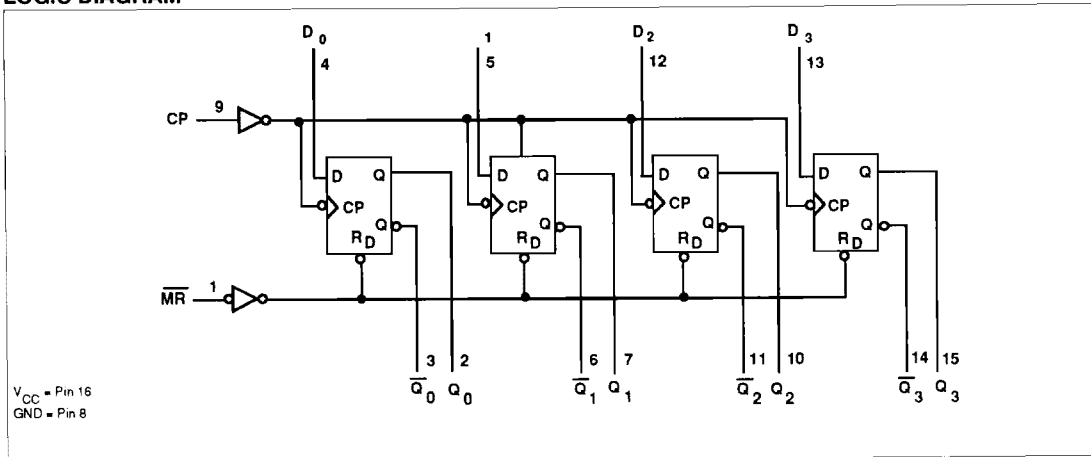
### LOGIC SYMBOL (IEEE/IEC)



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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
MR	CP	D	$Q_n$	$\bar{Q}_n$	
L	X	X	L	H	Reset (clear)
H	$\uparrow$	h	H	L	Load "1"
H	$\uparrow$	l	L	H	Load "0"

- H = High voltage level
- h = High voltage level one set-up time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Low-to-High clock transition
- X = Don't care
- $\uparrow$  = Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
$V_{CC}$	Supply voltage	-0.5 to +7.0	V	
$V_{IN}$	Input voltage	-0.5 to +7.0	V	
$I_{IN}$	Input current	-30 to +5	mA	
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to + $V_{CC}$	V	
$I_{OUT}$	Current applied to output in Low output state	40	mA	
$T_{amb}$	Operating free-air temperature range	Commercial range	0 to +70	$^{\circ}C$
		Industrial range	-40 to +85	$^{\circ}C$
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$	

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_{amb}$	Operating free-air temperature range	Commercial range	0	70	°C
		Industrial range	-40	85	°C

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			Min	Typ <sup>2</sup>	Max		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN.}, V_{IL} = \text{MAX.},$ $V_{IH} = \text{MIN.}, I_{OH} = \text{MAX.}$	$\pm 10\%V_{CC}$	2.5		V	
			$\pm 5\%V_{CC}$	2.7	3.4		
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN.}, V_{IL} = \text{MAX.},$ $V_{IH} = \text{MIN.}, I_{OL} = \text{MAX.}$	$\pm 10\%V_{CC}$		0.30	V	
			$\pm 5\%V_{CC}$		0.30		
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN.}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = 0.0V, V_I = 7.0V$			100	$\mu A$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX.}, V_I = 2.7V$			20	$\mu A$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX.}, V_I = 0.5V$	'F175		-0.6	$\mu A$	
			'F175A		-20		
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX.}$		-60	-150	mA	
$I_{CC}$	Supply current (total)	$V_{CC} = \text{MAX.}$	'F175		25	34	mA
			'F175A		22	31	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5V, T_{amb} = 25^\circ C$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test,  $I_{OS}$  tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS FOR 74F175

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	Min	Max	Min	Max		
$f_{MAX}$	Maximum clock frequency	Waveform 1	100	140		100		100		MHz	
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $Q_n$ or $\bar{Q}_n$		4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	3.5 4.0	8.5 10.0	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\bar{M}B$ to $Q_n$	Waveform 3	4.5	9.0	11.5	4.5	13.0	4.5	13.0	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\bar{M}B$ to $\bar{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	4.0	11.0	ns	

## AC ELECTRICAL CHARACTERISTICS FOR 74F175A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			
			Min	Typ	Max	Min	Max	Min	Max		
$f_{MAX}$	Maximum clock frequency	Waveform 1	140	160		125		110		MHz	
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to $Q_n$ or $\bar{Q}_n$	Waveform 1	3.0 4.5	4.0 6.0	6.5 8.5	2.5 4.0	7.5 9.0	2.5 4.0	8.0 10.0	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\bar{M}B$ to $Q_n$	Waveform 3	4.5	6.5	9.0	4.5	10.0	4.5	11.0	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay $\bar{M}B$ to $\bar{Q}_n$	Waveform 3	4.5	6.0	8.0	4.0	9.0	4.0	10.0	ns	

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## AC SETUP REQUIREMENTS FOR 74F175

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	Min		Max
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $D_n$ to CP	Waveform 2	3.0 3.0			3.0 3.0		3.0 4.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $D_n$ to CP	Waveform 2	1.0 1.0			1.0 1.0		1.0 1.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse width High or Low	Waveform 1	4.0 5.0			4.0 5.0		4.0 6.0		ns
$t_w(\text{L})$	<u>MR</u> Pulse width Low	Waveform 3	5.0			5.0		5.0		ns
$t_{\text{REC}}$	Recovery time <u>MR</u> to CP	Waveform 3	5.0			5.0		6.0		ns

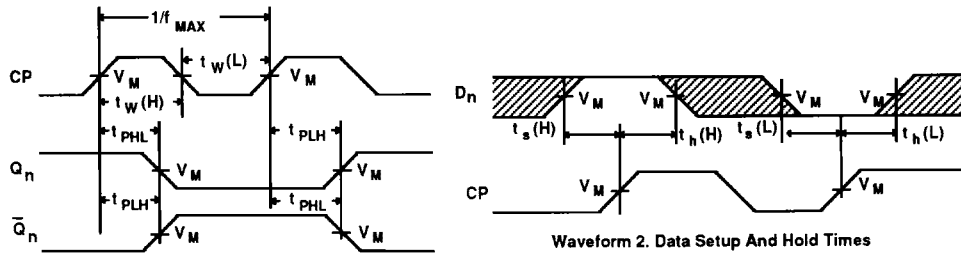
## AC SETUP REQUIREMENTS FOR 74F175A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = 5\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 5\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	Min		Max
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $D_n$ to CP	Waveform 2	3.0 3.0			3.5 3.5		4.0 4.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $D_n$ to CP	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse width High or Low	Waveform 1	3.0 4.0			3.5 5.0		4.0 5.5		ns
$t_w(\text{L})$	<u>MR</u> Pulse width Low	Waveform 3	3.5			3.5		4.0		ns
$t_{\text{REC}}$	Recovery time <u>MR</u> to CP	Waveform 3	4.0			4.5		5.0		ns

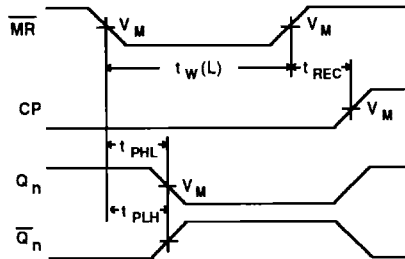
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## AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency

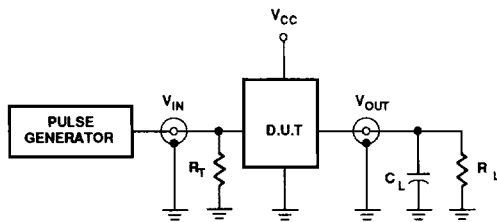


Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

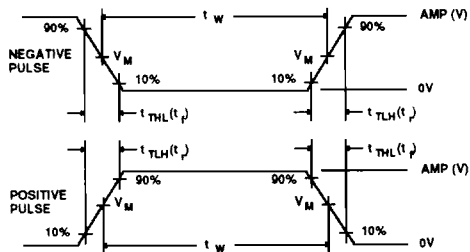
NOTE: For all waveforms,  $V_M = 1.5V$ .

The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

### DEFINITIONS

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1MHz	500ns	2.5ns	2.5ns